Hybrid Silicon DQPSK Receiver

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Abstract: We present a monolithic 50 Gb/s DQPSK receiver on hybrid silicon, consisting of delay interferometers, phase shifters, balanced InGaAs p-i-n photodetectors, and MIS capacitors. Preliminary measurements of stand-alone PDs show 23-28 GHz 3dB bandwidth.

1. Introduction

QPSK and DQPSK are becoming more prominent modulation formats due to their increased spectral efficiency compared to OOK and tolerance to chromatic dispersion [1]. QPSK receivers have the benefit of higher sensitivity, but require the use of a local oscillator. DQPSK receivers do not require a low linewidth laser or high speed signal processing for carrier phase estimation due to their differential detection scheme [2]. DQPSK receivers on silicon are of interest for their potential compatibility with low cost, high volume and mature CMOS processes [3].

2. Design

The DQPSK receiver consists of two MMI-based delay interferometers with four NiCr heater phase shifters, two balanced InGaAs p-i-n photodetector pairs, and four on-chip MIS (metal-insulator-semiconductor) capacitors. The mask layout is shown in Fig. 1 (a) and (b) is a photo of the device. The two 40 ps interferometers are to be biased at $\pi/4$ and $-\pi/4$ in order to receive the different signal quadratures.

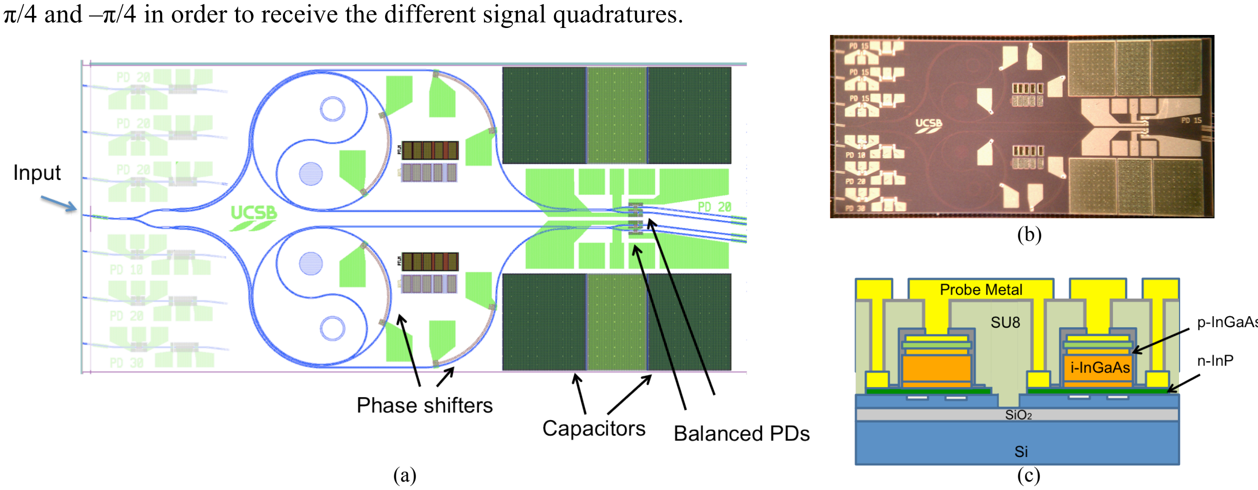

Figure 1. Mask layout of the DQPSK receiver (a). Waveguides are shown in blue, metal contacts are light green. The layout includes stand-alone single PD test structures on the left. Photograph of the receiver PIC (b) and details of the balanced p-i-n InGaAs PD structure (c).

The waveguide structure is SOI with a 0.7 µm waveguide height and 0.3 µm etch depth. The phase shifters are NiCr heaters 10 µm wide and 500 µm long. The balanced photodetectors shown in Fig. 1(c) have a similar structure as the single photodetector in [4], with a 0.5 µm thick intrinsic InGaAs absorber region. The photodiode lengths of 10, 15, 20, 25, 30 µm were chosen for 25 Gbaud operation considering RC and transit time limitations. The on-chip MIS capacitors have 3000 Å thick SiN as the dielectric, use the n-InP layer as the semiconductor, and are designed to be approximately 50 pF, as large as possible given the space constraints of the device.

3. Preliminary Results

Preliminary photodetector (PD) characterization, in terms of frequency response and receiver sensitivity, was done on stand-alone single photodetector test structures fabricated with the receivers, shown on the left side of Fig. 1 (b). The frequency response was measured with the LCA (Lightwave Component Analyzer) output coupled into the PD with a lensed fiber. The PD was contacted with a GSG RF probe and reversed biased through a bias tee. The RF signal from the PD was connected to the LCA through the bias tee. Fig. 2(a) shows the normalized response of the

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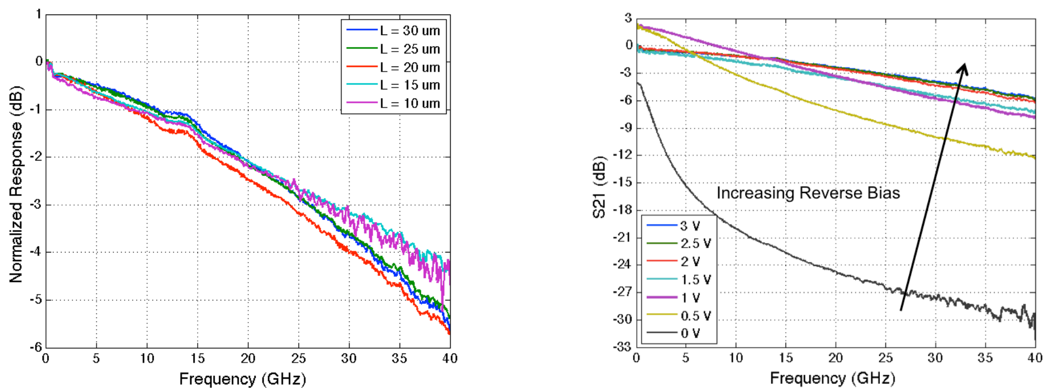
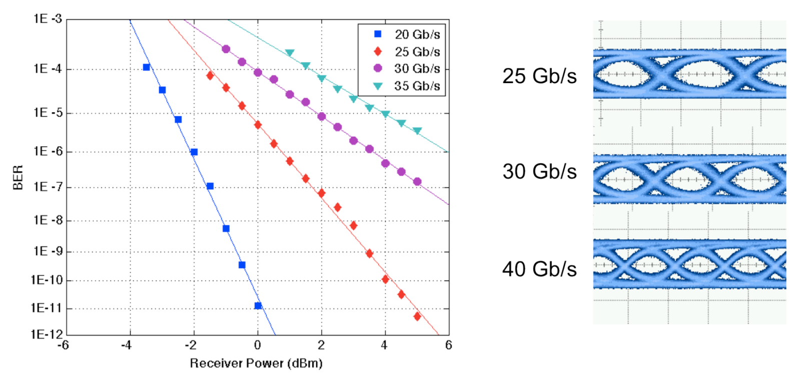
photodetectors of lengths 10-30 µm, with 3dB bandwidth ranging from 23 to 28 GHz. Fig. 2(b) shows the effect of increasing reverse bias on a 30 µm long photodetector.

To measure PD sensitivity, an NRZ-OOK signal with a PBRS 2^{31}-1 pattern was amplified by an EDFA, attenuated by a variable optical attenuator, and then coupled into the PD with a lensed fiber. The PD was reversed biased at -3V with a bias tee and the RF signal from the PD was sent through the bias tee to the BERT or scope. Fig. 3(a) shows the NRZ-OOK BER curves at 20, 35, 30, and 35 Gb/s, assuming a 10 dB coupling loss from fiber to chip, and receiver sensitivity of approximately -0.5 dBm at 20 Gb/s and 3.5 dBm at 25 Gb/s. Since the PD is neither preamplified nor postamplified, receiver sensitivity is low. Low sensitivity is also attributed to a small (<1µm) overlap of the p-metal layer and n-contact, causing a short that results in lower responsivity and a high dark current. The NRZ-OOK eye diagrams at 25, 30, and 40 Gb/s are shown in Fig 3(b) with 15 dBm of input power measured at the lensed fiber.



(a) (b)

Figure 2. (a) Normalized photodetector response for detector lengths L=10, 15, 20, 25, 30 µm at 3V reverse bias and (b) response varying reverse bias for detector length L=30 µm.



(a) (b)

Figure 3. (a) NRZ-OOK BER curves with a PBRS 2^{31}-1 pattern. The receiver power is the estimated power at the PD, assuming 10 dB coupling loss. (b) NRZ-OOK Eye diagrams at 25, 30, and 40 Gb/s (20 ps/div) with 15 dBm at lensed fiber (5 dBm to PD assuming 10 dB coupling loss)

3. Conclusions and Future Work

Preliminary photodetector measurements performed on stand-alone single photodetector test structures verify PD operation at 25 Gb/s. Future work includes characterization of the delay interferometer, balanced photodiodes, and the demonstration of this device as a receiver with 50 Gb/s DQPSK data.

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4. References

[1] Winzer, P. J., Essiambre, R.-J., "Advanced Modulation Formats for High-Capacity Optical Transport Networks," *Journal of Lightwave Technology,* , vol.24, no.12, pp.4711-4728, Dec. 2006

[2] Doerr, C.R.; Long Chen, "Monolithic PDM-DQPSK receiver in silicon," *Optical Communication (ECOC), 2010 36th European Conference and Exhibition on* , vol., no., pp.1-3, 19-23 Sept. 2010

[3] H. Park, A. W. Fang, D. Liang, Y.-H. Kuo, H.-H. Chang, B. R. Koch, H.-W. Chen, M. N. Sysak, R. Jones, and J. E. Bowers, *Advances in Optical Technologies,* Article ID 682978, 2008

[4] H.-H. Chang, Y.-H. Kuo, R. Jones, A. Barkai, ,J. E. Bowers, Integrated Hybrid Silicon Triplexer, Optics Express, Vol. 18, Issue 23, pp. 23891-23993 (2010)