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Sub-wavelength Metal Gratings for In-plane Lasers and Integrated Optical Elements

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in

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by

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ABSTRACT

Sub-wavelength Metal Gratings for In-plane Lasers and Integrated Optical Elements

by

Erica Lively

Sub-wavelength periodic metal structures are currently being explored by many branches of photonics for enhanced light control on the nano-scale. Metal holes or slits have shown promise in plasmonic application areas like mirrors, couplers, waveguides, and lenses. These structures are also beginning to making a large impact on many emerging areas in photonics such as slow light, left-handed materials, and sensing. While metal and semiconductor integrated devices have rapidly advanced in sophistication over the last decade, few have yet to address the major challenges associated with transitioning from individual devices that demonstrate basic, physical operation to devices with potential for current and near-future telecommunications applications. Outstanding novel devices using metals have been presented, but they are missing key features that allow them to be integrated into photonic circuits. As we begin bridging the gap between simple, passive devices fabricated with traditional optical lithography and basic liftoff techniques to more sophisticated, sub-wavelength scale active devices, we focus on sub-wavelength metal gratings with design choices made to favor integration, both with respect to current state of the art optical components and fabrication on the nano- and micro-scale.

In this dissertation, we present a theoretical and experimental study of potential applications of sub-wavelength metal gratings in photonic integrated circuits. We consider on-chip slow light functionality and determine that the most achievable near-term impact of sub-wavelength metal gratings can be made in the area of on-chip, in-plane metal mirrors. We demonstrate the operation of a distributed Bragg reflector (DBR) laser with two metal grating mirrors operating on an InP-based materials platform. We account for future design considerations of scale and polarization to show that there is strong potential for integrating sub-wavelength metal gratings into current photonic integrated circuits.

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Chapter 1

Introduction

1.1 Photonic Integrated Circuits

For the majority of the history of optical networks, individual components in an optical system have been discrete modules that are linked together. Transmitters, modulators, and receivers have been interconnected with optical fibers aligned to each of the input and output optical data ports. Traditionally, this has required a large number of fiber alignments, which leads a large amount of time and money spent packaging fibers. Additionally, each on-chip to fiber transition creates coupling loss, which eventually adds up to increased noise throughout the system and decreased overall system performance. With the addition of each individually packaged component comes an increase in the size of the system eventually leading to a single optical system requiring a very large amount of space. When you take into account the space required for supporting electronics and temperature control, this method of building a system from discrete components scales poorly.

As the demand grows for higher data rates and more functionality from optical circuits, it becomes necessary to find a way to integrate many optical components into a single device. Developments in InP-based materials and processing allow for the

principal devices of optical systems to be combined onto a single chip, known as monolithic integration. Years of refining InP-based integration technologies have lead to single optical chips with immense capabilities. For example, Figure 1.1 shows the monolithic tunable optical router (MOTOR) chip developed at UCSB in 2010. This single chip acts as the switch fabric for an optical router. It has over 200 integrated functional elements and a total potential data capacity of 640 Gbps[1].

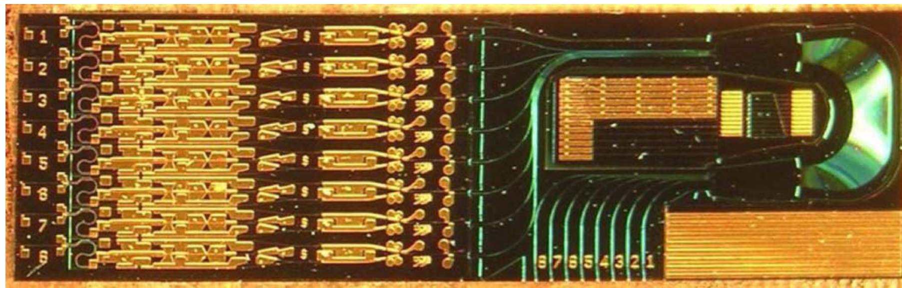

Figure 1.1 MOTOR chip developed at UCSB with over 200 integrated functional elements[1].

Figure 1.2 shows a coherent QPSK receiver developed by the Infinera Corporation in 2011. It has 10 optical channels and a reported total data capacity of over 1 Tbps[2]. In 2011, it was the largest reported photonic integrated circuit.

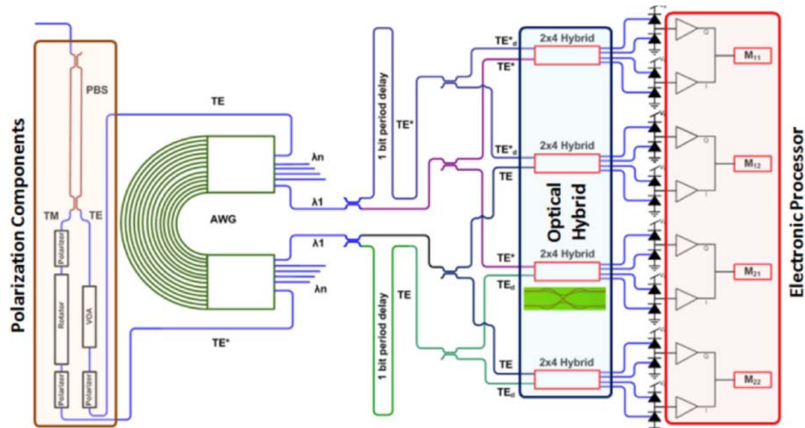

Figure 1.2 Coherent QPSK receiver developed by Infinera with a total data capacity of over 1 Tbps[2].

These PICs demonstrate that on-chip integration has revolutionized our approach to optical systems. Enhance system reliability and a small footprint are now the standards set by large-scale integrated PICs. There is still significant room for PICs to grow using current technologies, but as we attempt to push the capabilities of systems on a chip further and further, we must also understand and address their limitations.

1.2 Methods of Scaling Photonic Integrated Circuits

The most common method used to scale the performance of photonic integrated circuits is to add more components to a single chip. By packing more components onto a single PIC to create multiple replicated data channels, one can achieve impressive system performance, as demonstrated by the two large scale PICs in the previous section. However, as we begin scaling photonic integrated circuits this way, there are many challenges that develop as we add more and more components to the

system, just as with optical systems composed of discrete components. For monolithically integrated PICs, some of the issues that arise are increased packaging requirements, decreased processing yield, and increased power consumption.

As devices are scaled up in size and more optical channels are added, device packaging and fiber coupling becomes increasingly complicated. Additionally, as the PIC footprint is increased, the likelihood of one or more of the on-chip components being damaged during processing goes up. This requires larger numbers of devices to be processed in order to account for those that fail or suffer poor performance because of fabrication issues. Finally, as single PICs have more active components, the total power consumption to power and cool the chip also increases[3]. Compounding these issues can result in a rapid cost increase per PIC as the chips become larger.

While the current large-scale PICs boast impressive system performance, future generations of photonic integrated circuits will require novel approaches to the existing method of scaling on-chip components. There are some technologies that aim to solve these issues that are rapidly maturing. Silicon photonics presents a promising approach by capitalizing on the abundance and ubiquity of silicon to reduce the overall cost of individual components[4]. Advanced modulation formats like dual quadrature phase shift keying (DQPSK) aim to increase data capacity of a single PIC with very little increase in footprint[5]. But a less explored approach that shows potential for improving the miniaturization and functionality of photonic integrated circuits is the integration of metals with semiconductor and dielectrics to form highly dense, highly functional photonic integrated circuits.

1.3 Metal-Semiconductor-Dielectric Integration

Metals have been integrated into photonic circuits for a hugely varied set of applications. Metal slits or gaps have been proven to be good electric field concentrators used to act as traps[6]. Patterned metals have also been demonstrated as electromagnetic field cloaking devices [7]. Metal gratings have been demonstrated as plasmonic waveguide couplers, planar waveguide sensors, and lenses on VCSELs[8-10]. Similar structures on the sub-wavelength scale have also been theorized to be able to make impacts in slow light, but have not yet been experimentally proven[11].

Another promising application in metal-integrated photonic devices is the nano-cavity laser demonstrated in 2009 at TU-Eindhoven[12]. Figure 1.3 shows an active semiconductor stack patterned into a deeply etched ridge and coated in silver. This laser has many limitations in its current form, namely that the only way to measure light generated by the laser is to collect scattered light out of the bottom. This laser holds exciting promise for photonic circuit miniaturization, but it is not currently an integrable device. In order for it to have potential for in-plane optical circuit uses, light must be transmitted to other components on the same chip. However, when this limitation is addressed, these lasers may hold promise for low power PICs with very small footprints.

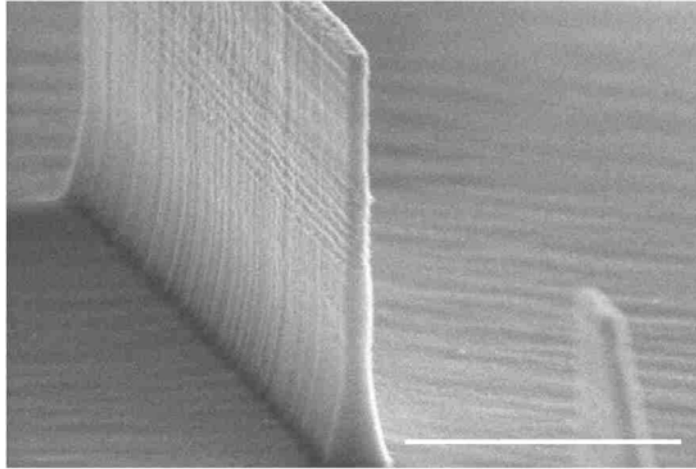

Figure 1.3 Metal-coated nano-scale laser cavity developed at TU-Eindhoven in 2009[12].

Individual optical elements have been demonstrated using metals but additional design components are necessary to further integrate these individual pieces into a photonic circuit. This research is still in its infancy and there are many steps that must be taken before a fully functional PIC can be realized using this technology. However, the potential benefits of such reduced scale circuits hold enough promise to warrant further investigation.

1.4 Preview of This Work

In this dissertation, we explore the integration of sub-wavelength scale metal gratings as optical circuit elements. While this design space is somewhat nebulous, we focus on developing fabrication methods that can bring metal grating based devices out of the theory and simulation domain in order to realize them as measurable devices. Additionally, our motivation is to expanding the current demonstrated functionality of

metal grating devices while keeping in mind the feasibility of developing a working prototype. There are certainly many other ways to design on-chip slow light devices or nano-scale lasers, but in this dissertation, we focus on understanding how sub-wavelength scale metal gratings can be used to tackle future integration and functionality challenges for metal-semiconductor-dielectric photonic integrated circuits.

This work is presented as follows. Chapter 2 discusses the background and theory of sub-wavelength scale metal gratings and presents finite element method (FEM) and finite difference time domain (FDTD) simulations for potential on-chip slow light applications. Chapter 3 presents the development of a flexible, platform independent fabrication method for metal gratings that allows us to test designs that have only been previously theorized. After preliminary testing and analysis, we determine that a realistic near-term demonstration of the functionality of integrated metal gratings is to use them as mirrors for in-plane lasers. Chapter 4 presents the design considerations and methods for integrating metal gratings as a first proof-of-concept approach to laser integration. Chapter 5 discusses the fabrication of the devices and focuses on challenges that must be overcome when integrating many micro-scale and nano-scale features into a single device. The results of device performance testing and lessons learned are presented in Chapter 6. Finally, Chapter 7 presents a summary of the dissertation and reflects on the direction and design considerations of future sub-wavelength metal grating integration.

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Chapter 2

Background and Theory of Sub-wavelength Metal Gratings

The optical properties of patterned metal structures have been explored for a very wide array of applications, as previously discussed in Section 1.3. Because the uses of patterned metals are so varied, we will focus on three principle properties that have shown promise for using patterned metals for photonic circuit integration. In order to better determine how patterned metals can help us expand optical circuit functionality, we'll discuss how metals can be used for their high reflectivity, plasmon response, and their behavior as metamaterials.

The most straight forward property of metals that is employed at optical wavelengths is their high reflectivity. The high reflectivity of metals allows optical cavities to be created in a smaller amount of space, but it does often come with high losses. It is not uncommon for metals to have a real index less than one. This high reflectivity comes with a high imaginary index value, indicating high loss values. Metal holes or gaps have been demonstrated as effective electric field concentrators or traps[1], as well as capable of enhancing off-chip light coupling[2]. Some of the more effective uses of metals in optical circuits combine the high reflectivity of metals with an additional property, the plasmonic response.

Surface plasmons occur as collective excitations of electrons at the interface between a metal and a dielectric or semiconductor[3]. These excitations behave like a traveling wave at the interface with the field distribution shown in Figure 2.1(a). Surface plasmons can be excited by photons at an interface if there is a perturbation like a grating at the metal-dielectric interface. And likewise, optical energy can be recovered from plasmons with the same grating perturbation[4]. One effect of surface plasmons that would be useful to exploit in modern photonic integrated circuits, is their group velocity distribution. The group velocity of a wave is defined by the relationship between ω, the frequency, and k, the wavevector. Equation 2.1 show that the group velocity of a wave is defined by the rate of change of ω with respect to the rate of change of k, meaning that if ω changes very little, while k continues to increase, the group velocity approaches zero.

$$v_g = \frac{\partial \omega}{\partial k} \tag{2.1}$$

Figure 2.1(b) shows that, as we look at the wavevector, k, with respect to frequency, ω, plasmons have a distinct non-linear band bending as we approach higher ω vs. k values, indicating that very low group velocities could be achieved[5].

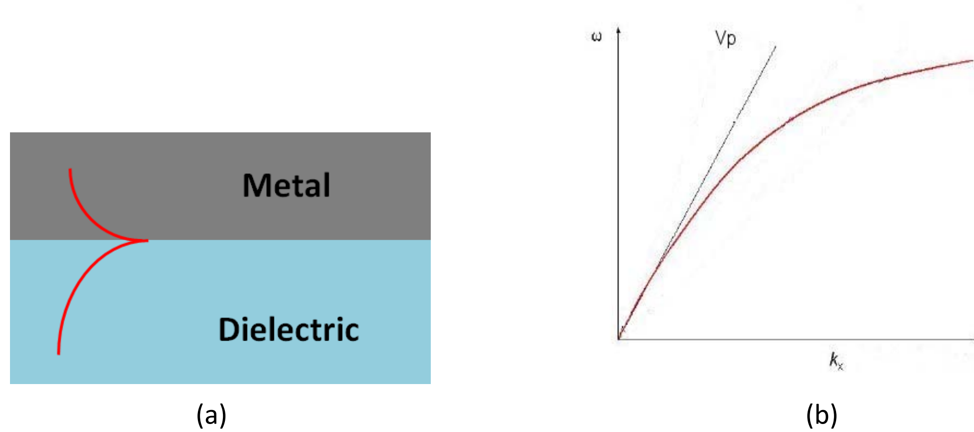


Figure 2.1 (a) Plasmon excitation at a metal dielectric interface. (b) Theoretical dispersion curve of surface plasmons.

Photonic integrated circuits often rely on optical delays. Short delays are used to align phase in DQPSK systems[6] or bits in on-chip WDM systems[7], and long delays are needed to buffer entire optical packets[8]. On-chip delays often take up significant amounts of space on the chip, but by exploiting this group velocity reduction in plasmonics, we could potentially create shorter on-chip delays. However, one main issue with integrating plasmonic effects into PICs designed to operate at telecommunications wavelengths ranging from 1300nm-1600nm, is that the optical wavelength corresponding to the plasmons generated by common metal-dielectirc combination typically ranges from 300nm-500nm[9]. This presents a huge problem if we ever hope to use the plasmonic group velocity reduction in optical circuits at telecommunications wavelengths. However, the final optical property of patterned metals, acting as metamaterials, will present a solution to this problem.

A metamaterial is generally defined as a material that exhibits properties not found in the bulk material when patterned with a periodicity smaller than the optical wavelength[10]. Some fantastic demonstrations of metamaterials have been shown in the last 5 years, such as using patterned metals to electromagnetically cloak objects[11]. It has also been predicted that metal gratings with a sub-wavelength periodicity will mimic the surface plasmon response at optical telecommunication wavelengths[12]. The following sections discuss this effect and the possibility of integrating sub-wavelength metal gratings into an optical PIC.

2.1 Sub-wavelength Metal Gratings

When we first being talking about the optical properties of gratings, the most natural inclination is to begin thinking about their transmission and reflection properties. Most of the familiar uses of gratings rely on their wavelength selectivity, as well as their ability to diffract and disperse light. These grating properties will become very crucial later in this dissertation, but for now, as we focus on the metal grating acting as a metamaterial, we will address the guided modes of the grating. Well-documented theory has shown us that if we have a very simple metal grating suspended in air with the periodicity, a, and gap width, d, the guided modes of the grating will behave as if the grating is a dielectric slab with the index of refraction, n, being a divided by d, and a height of the grating height, L, divided by n[13]. This means that, for a perfect electrical conductor, the resulting metamaterial effect is

defined entirely by the geometry of the grating. Figure 2.2 gives a schematic of the grating geometry and resulting dielectric slab.

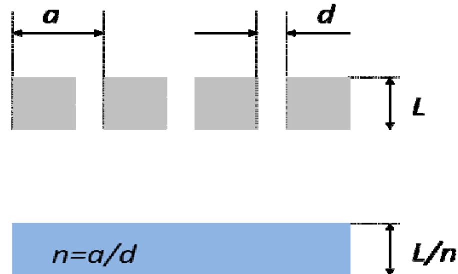


Figure 2.2 Metal grating geometry and resulting dielectric slab as predicted by metamaterial theory.

This metamaterial effect indicates that we could create a very high index material simply by choosing the proper grating geometry. This presents a nice solution to our previous desire to capitalize on the low group velocity of surface plasmons. However, this condition only occurs for TM polarized light with the electric field aligning in the y-direction, parallel to the grating. Figure 2.3 shows the band diagrams in blue of the guided modes in the perfect electrical conductor grating.

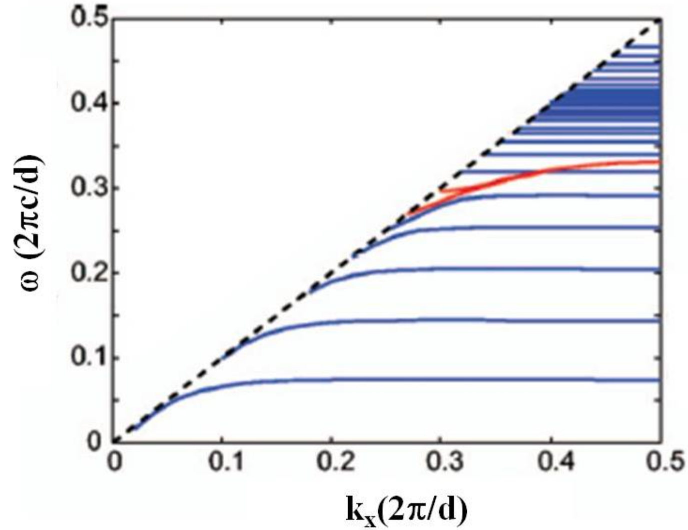


Figure 2.3 Band diagrams of guided modes supported in patterned metal grating developed by P. Catrysse, *et.al.*[14]

This initial theory is based on a perfect electrical conductor with no loss. This is an unachievable ideal case scenario. The predicted band diagrams for guided modes in a grating made from a real, lossy metal are shown in red[14]. While they do not have the same rapid band flattening of the perfect electrical conductor curves leading to reduced group velocities, there is still an observable amount of band bending. Using this preliminary metamaterial theory, we will try to determine if it might be possible to transform these suspended metal gratings into an integrable optical element.

2.2 Platform Integration

Further study is needed to determine if the theoretical gratings isolated in space will likely exhibit the same behavior if they are integrated onto a semiconductor material

platform. As we begin to conceptualize how we might take metal gratings from the theoretical domain into a form that can be fabricated and tested, we want to focus on how these structures could feasibly be integrated with a real photonic circuit. We begin this study by creating a very simple integrated version of the gratings. Because most highly functional PICs are currently fabricated on an InP platform, we will stay within that material reference framework. For the basic simulation prototype, we choose an InP substrate with an InGaAsP waveguide layer etched into a ridge, followed by the gratings on top of the waveguide. Figure 2.4(a) shows a three dimensional image of the proposed structure, while Figure 2.4(b) shows a grating cross-section of the structure. We will use this integrated grating prototype as a baseline for our simulation study described in Section 2.3.

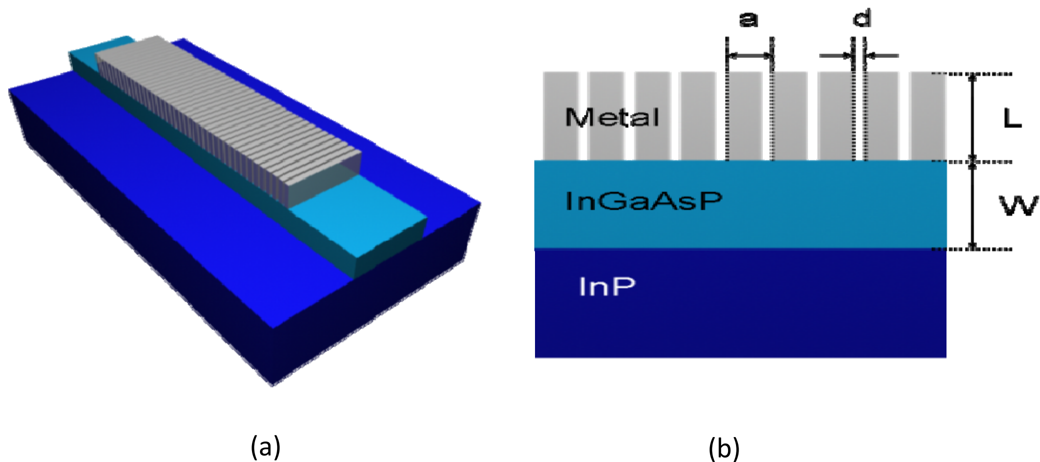


Figure 2.4(a) Three dimensional image of the integrated grating structure. (b) Grating cross-section of the structure.

2.3 Simulation of Metal Gratings

In order to design an integrated grating, we will use two different simulation techniques to predict the behavior of sub-wavelength metal gratings when they are integrated onto a simple InP-based semiconductor platform. We'll begin by using the finite element method (FEM) to simulate whether the integrated grating still shows the plasmon-like response predicted by the suspended grating. Next we'll use the finite difference time domain (FDTD) method to see if we can simulate the delay of an optical pulse based on the results from the FEM simulations. Both simulation methods and results will be discussed in the following sections.

2.3.1 Finite Element Method (FEM) Simulations

In the most general sense, the finite element method is a numerical procedure for obtaining solutions to boundary value problems. An entire continuous domain is replaced with a number of subdomains that can be represented by simple interpolation functions. The solution of the entire system is approximated by a finite number of unknown coefficients. The four steps of the finite element method are as follows: subdivide the domain, select the interpolation function, create a system of equations, and solve the system of equations. Using these four steps, any arbitrary geometry can be implemented with this method as the solution for each subdomain is only dependent on its neighboring domains[15]. For our application, we'll take advantage of the periodicity of our grating structure and use Bloch functions to only simulate over one period of the grating, greatly reducing our simulation time[16].

Figure 2.5(a)-(c) shows how the grating unit cell is subdivided into a solution mesh for the finite element method. Figure 2.5(a) is the single unit cell of the grating we have chosen to simulate. Figure 2.5(b) show the FEM mesh of our unit cell. Note that the mesh is more dense around sharp edges and the material interfaces. Figure 2.5(c) is a closer view of the FEM mesh showing the defined subdomains, *a* through *d,* and their conjoining notes, 1 through 6. This mesh determines the set equations that will be solved to determine the modes supported by our defined structure. Because we are interested in guided modes and not radiation or scattering modes, we will define our system of equations as an eigenvalue system.

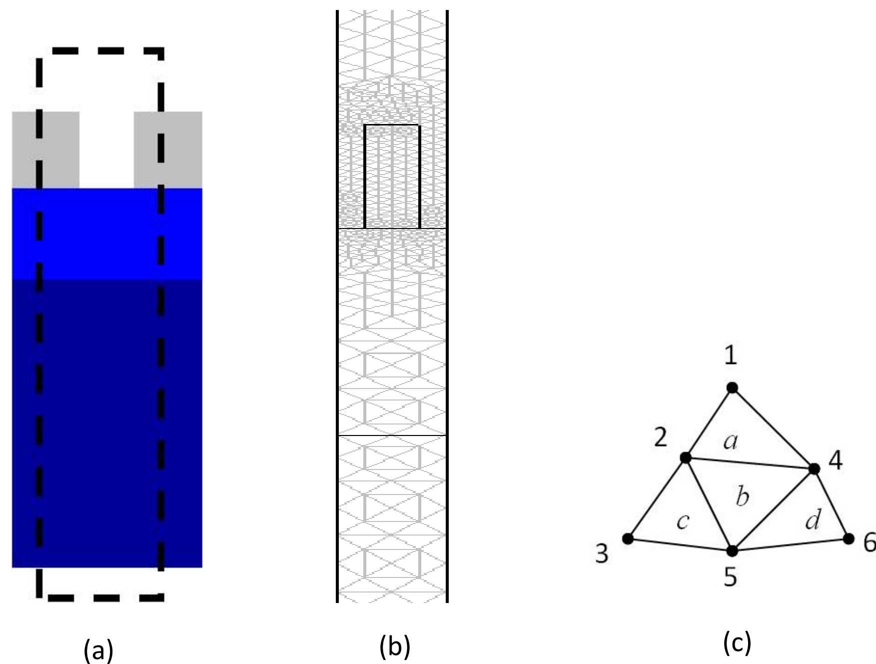


Figure 2.5 (a) Grating unit cell for FEM simulation. (b) Grid defined using FEM to establish subdomains to be solved (c) Closer view of FEM subdomains and nodes.

Once the FEM simulation is complete, we can analyze the eigenvalue solutions. Figure 2.6 shows four separate, graphical mode solutions for this simulation. The solution on the left has the lowest wavevector, *k*, value. Moving to the right, each solution has a slightly larger *k* value. We can see that as *k* increases, the intensity of the mode becomes more and more confined to the grating. This shows us that as we integrate the grating onto a waveguide platform, the confinement of the supported modes will vary between the waveguide and the grating, and will likely overlap with both the grating and waveguide.

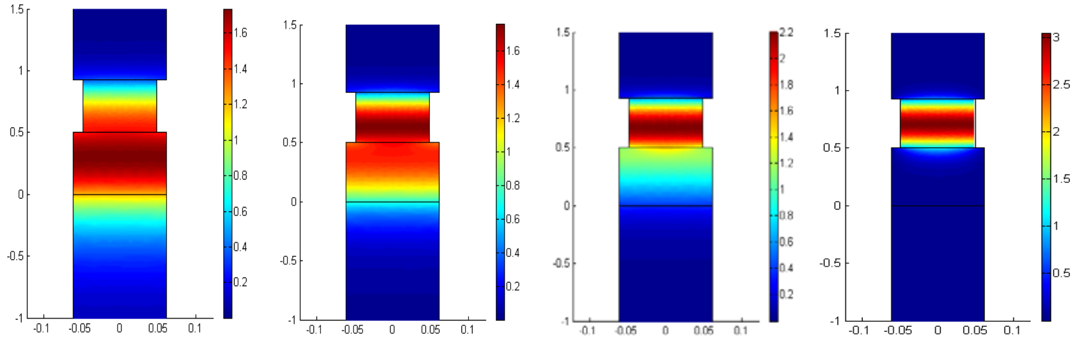


Figure 2.6 Four graphical mode solutions for our defined unit cell with increasing k values from left to right.

After we visually confirm that the mode solutions to our unit cell make sense, we can plot the ω vs. *k* relation of these modes. Figure 2.7 shows the dispersion relationship with ω normalized to *a*, the grating period, divided by *c*, the speed of light, and *k* normalized to *a* divided by pi. The blue trace on this plot shows us that there is one guided mode that demonstrates the plasmon-like band bending characteristic of group velocity reduction. We see that this band bending occurs only

at high k values. From the previous graphical mode plots in Figure 2.7, we know that the high k values correspond to high field confinement in the grating. This conclusion makes sense because we expect the group delay effect to result from mode interacting with the grating and it will likely be the strongest when the optical mode is highly confined to the grating.

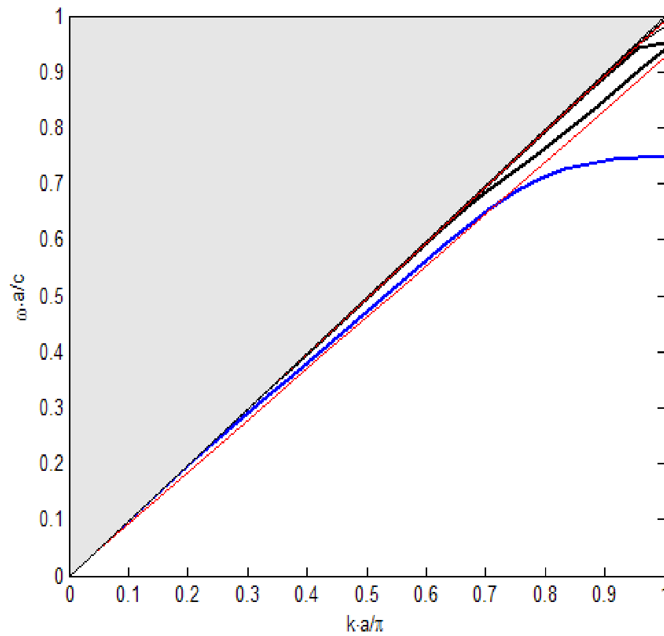


Figure 2.7 Band diagram plot of guided modes in designated FEM unit cell. Blue trace shows band bending characteristic of plasmon-like response.

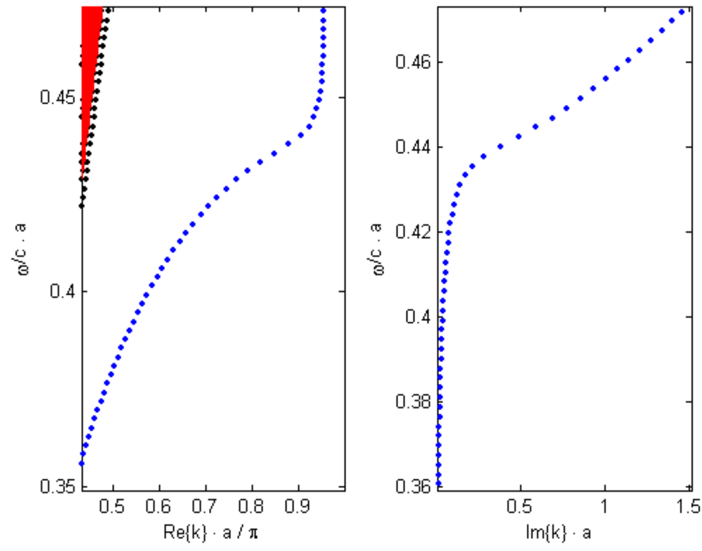
The previous simulations were conducted under the condition of modeling the metal as a perfect electrical conductor. If we now model the metal as a real conductor, we can further test the potential to integrate sub-wavelength metals with InP-based waveguides to achieve slow light. We will use the Drude model to simulate a real metal as it is widely regarded as a very accurate model in the optical domain[17].

Equation 2.2 gives the mathematical expression of the Drude model to calculate the dielectric constant of metals at optical frequencies.

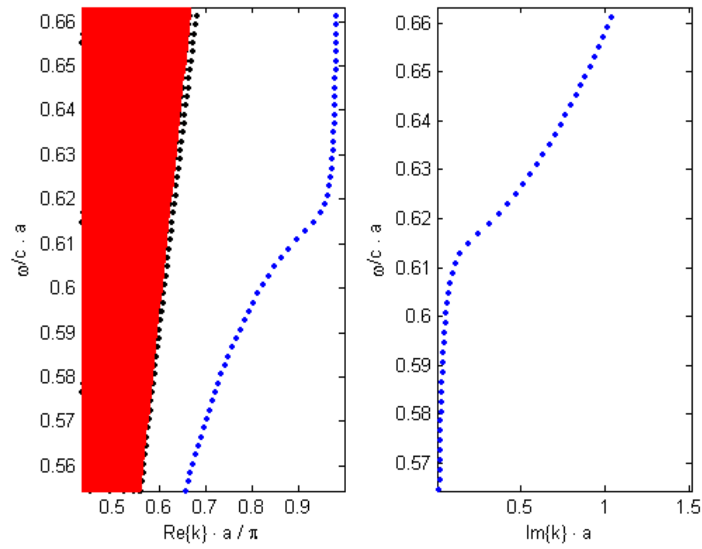
$$\varepsilon(\omega) = 1 + \frac{\omega_p^{\ 2}}{\omega(\omega + i\omega_c)} \tag{2.2}$$

After re-running the simulations to account for a real metal, we observe that the band bending effects seen with a perfect electrical conductor are still present, but they are not as strong. Figure 2.8 shows the real and imaginary band diagrams of the guided modes for a grating with (a) a periodicity, *a*, of 100nm and a gap, *d*, of 10nm and (b) a periodicity, *a*, of 150nm and a gap, *d*, of 10nm. In Figure 2.8(a), we can see that the band bending is more gradual than the perfect electrical conductor case and does not approach the same flatness. However, the effect is still present in the model with a real metal indicating that reduced group velocities or slow light could be achieved. The structure simulated for Figure 2.8(b) has a smaller *a/d* ratio than Figure 2.8(a), and we observe an even smaller band bending effect. Again, the plasmon-like response is still observable in the model, and this reaffirms the earlier theory that the geometry of the grating would determine the group delay effects.

Using the finite element method, we have shown the theoretically predicted effects of a sub-wavelength metal grating suspended in air can also be observed in a sub-wavelength metal grating integrated on top of a simple InP-based waveguide platform. Next, we will use the finite difference time domain (FDTD) method to simulate a pulse transmitted through the grating to determine if the group delay effect predicted by the FEM simulations can be observed.



(a)



(b)

Figure 2.8 shows the real and imaginary band diagrams of the guided modes for a grating with (a) a periodicity, *a*, of 100nm and a gap, *d*, of 10nm and (b) a periodicity, *a*, of 150nm and a gap, *d*, of 10nm.

2.3.2 Finite Difference Time Domain (FDTD) Simulations

The finite difference time domain (FDTD) simulation method is based on gridding an entire structure with equally sized grid spacing in each dimension and then stepping through the grid. The differential divergence and curl equations are interpolated to find the field values in a grid. Unlike the finite element method, where the mode solutions are simultaneous, the field solutions in each grid depend on the compounded solutions of the previous steps[18]. FDTD simulation is performed over an entire device structure, not a single unit cell, so it is good for visualizing radiation and scattering loss, as well as, determining coupling strength between the lower InGaAsP waveguide and the metal grating. Figure 2.9 shows a uniform two dimensional x-y grid defined over the integrated grating for FDTD simulation.

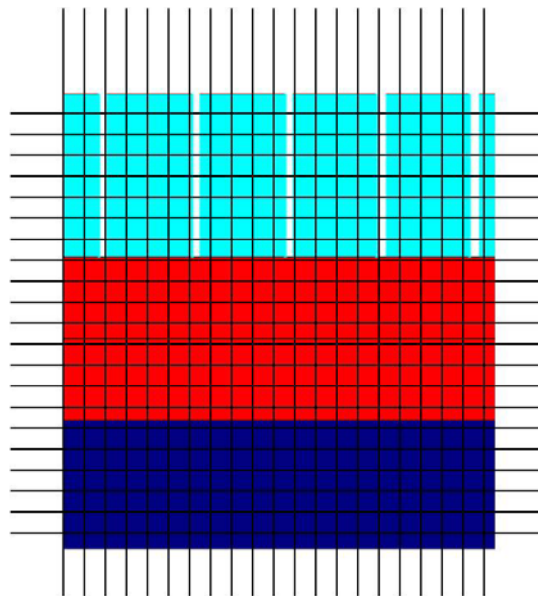


Figure 2.9 A uniform two dimensional x-y grid defined over a portion of the integrated metal grating structure for FDTD simulation.

We began our FDTD simulations by sending a very short pulse, just two wavelengths, through ten metal grating periods. The mode shape is defined as the fundamental mode of the InGaAsP waveguide without the grating. Figure 2.10(a) shows the graphical representation of the field as the pulse is traveling through the integrated grating structure. We can see that part of the field is confined to the grating and part is confined to the waveguide. There is also some scattering and radiation as the mode transitions between the fundamental waveguide mode and one that is coupled between the waveguide and the grating. Figure 2.10(b) shows a plot of the pulse power after the pulse has been transmitted through all ten periods of the grating compared to the power measured after the same pulse has traveled the same distance through the waveguide without an integrated grating. We can see that the pulse that encountered the grating is splitting into two pulses. Comparing field profile in Figure 2.10(a) and the output power measured in Figure 2.10(b), we believe that part of the input field is being coupled into the metal grating and is being slowed while part of the pulse continues to be transmitted through the waveguide with little effect from the grating.

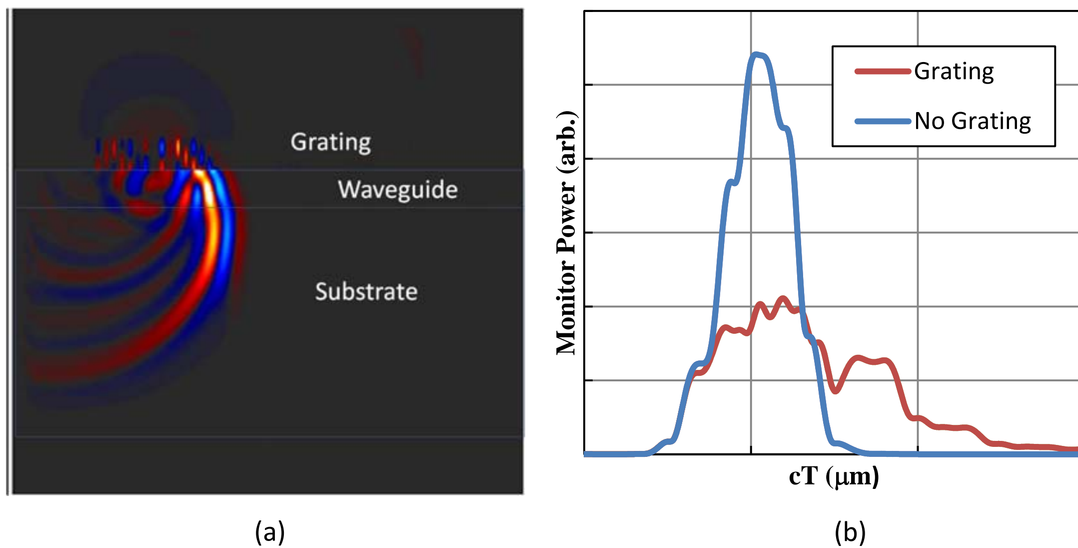


Figure 2.10(a) The field as the pulse is traveling through the integrated grating structure. (b) The pulse power after the pulse has been transmitted through the grating compared the waveguide without an integrated grating.

After this preliminary FDTD simulation, we see that it is possible to simulate a group delay in part of an optical pulse transmitted through a sub-wavelength metal grating integrated onto an InP-based waveguide platform. In order to more fully characterize what we would expect to see in a more feasible on-chip situation, we launch a pulse into the waveguide, next, the pulse encounters a 30 micron long metal grating, and finally, the pulse exits the grating where a monitor captures the total power and field overlap of the exiting pulse compared with the launched pulse. Figure 2.11 shows three cases for pulse transmission: (a) waveguide with no grating, (b) waveguide with a 30 um long grating, and (c) waveguide with a 30 um long shorted grating. The shorted grating has a strip of metal connecting all of the grating pillars. The shorted grating test case was chosen to address grating fabrication methods presented in Chapter 3.

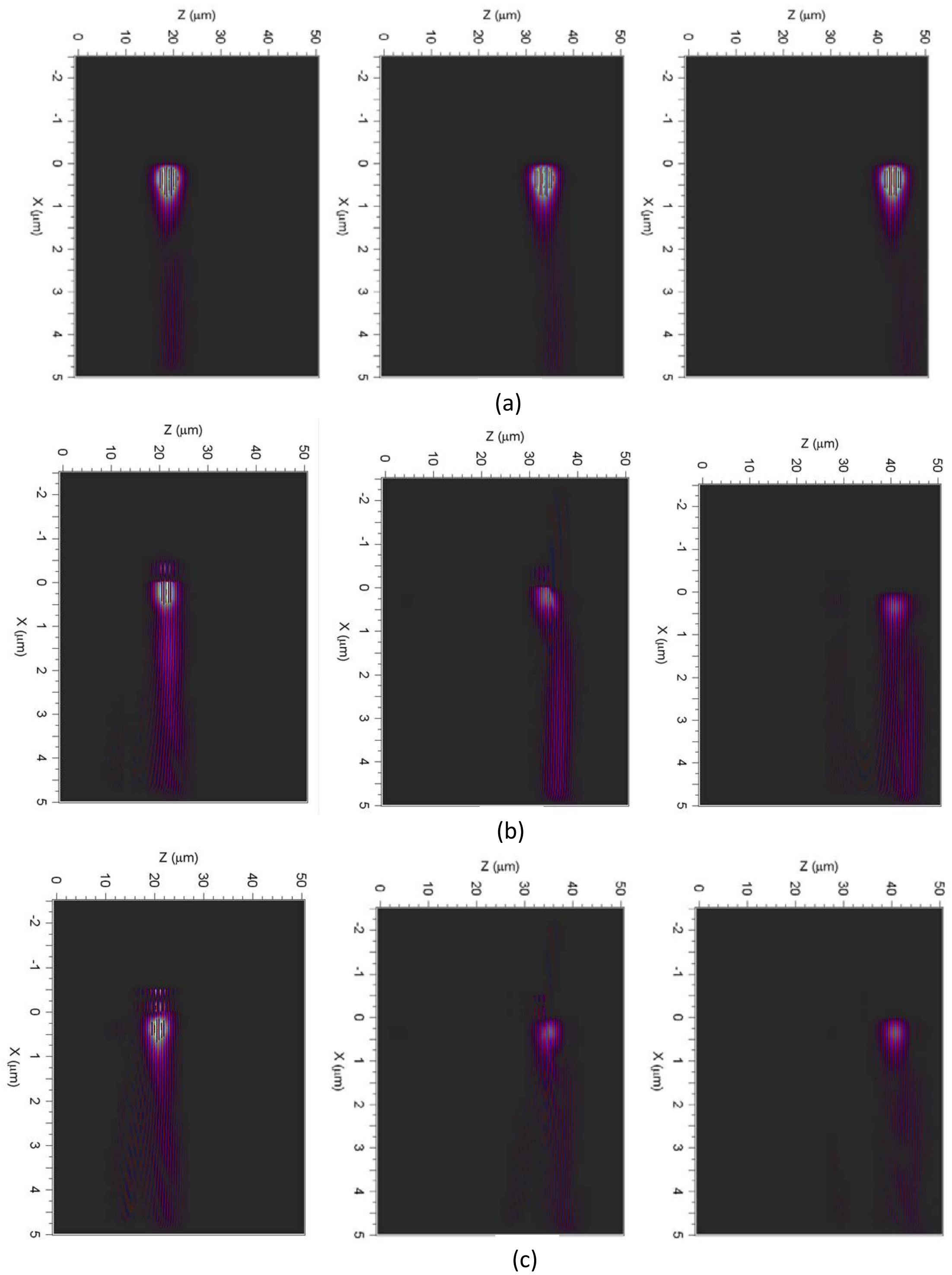
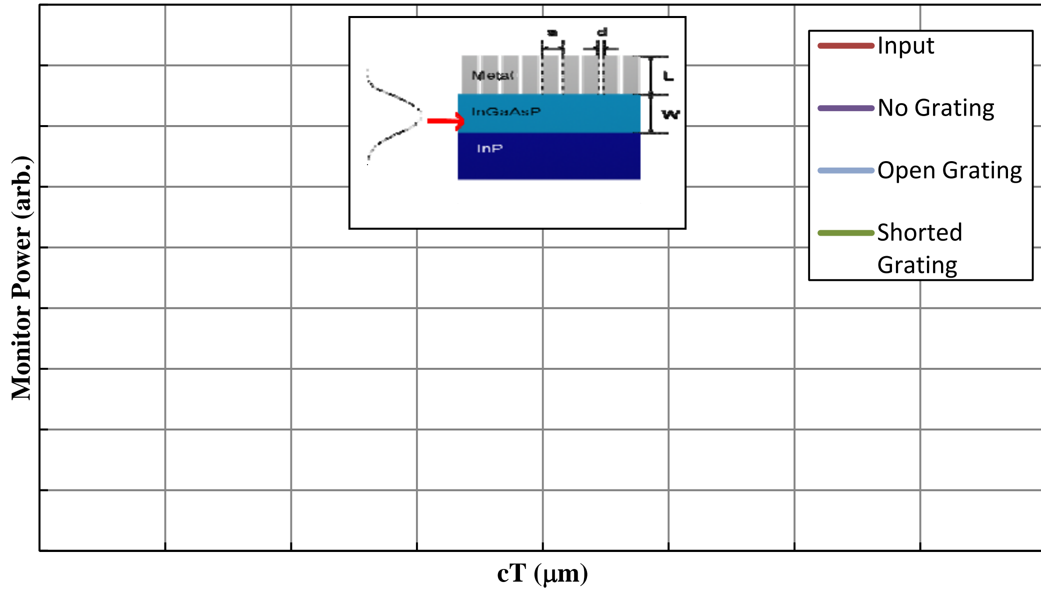


Figure 2.11 Three cases for pulse transmission: (a) waveguide with no grating, (b) waveguide with a 30 um long grating, and (c) waveguide with a 30 um long shorted grating. The first panel for each case shows the pulse after it has entered the grating (or location of grating), the second panel shows the pulse exiting the grating (or location of grating), and the third panel shows the transmitted pulse.

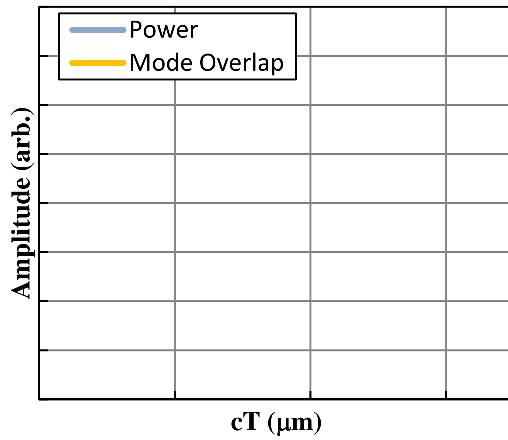
In Figure 2.11(a), we see that the pulse is transmitted through the waveguide with no disturbance, as expected. Figure 2.11(b), the case with our standard integrated grating, shows that some light is lost to radiative substrate modes as the fundamental waveguide mode couples into the grating mode. More light is again lost to radiation as the pulse exits the grating. We can also see that some of the transmitted pulse is reflected back through the grating. The results from Figure2.11(c), the case with the shorted grating, look very similar to the results from the standard grating in that light is lost to radiative and substrate modes. For this case, we can also see that a higher order mode is excited in the grating due to additional field reflections from the top, but the resulting transmitted pulse is very similar to that of the standard grating case.

Figure 2.12 shows the results of the power and field monitors, which as measure or detect field strength at user designated points in the simulation, for each case and allows us to compare the transmitted pulses. In Figure 2.12(a), we can see that the pulse transmitted through the waveguide with no grating is not distorted. This is expected since the pulse launched was the fundamental guided mode of the waveguide structure. We can also see from this figure that both of the pulses transmitted through the different gratings are distorted and have lost approximately two thirds of their launch power. The pulse transmitted through the standard, open grating is wider than the one transmitted through the shorted grating. However, both appear to be the superposition of two pulses. Figures 2.12(b-c) show us that, in fact, when we compare the mode overlap monitor to the total power monitor for both of the grating cases, the resulting pulse transmitted through the grating is a combination

of the delayed input pulse and substrate or radiative modes that were not coupled to the grating mode. This leads us to conclude that while, the transmitted pulse has been distorted, a portion of the light has been delayed demonstrating the predicted slow light response.



(a)



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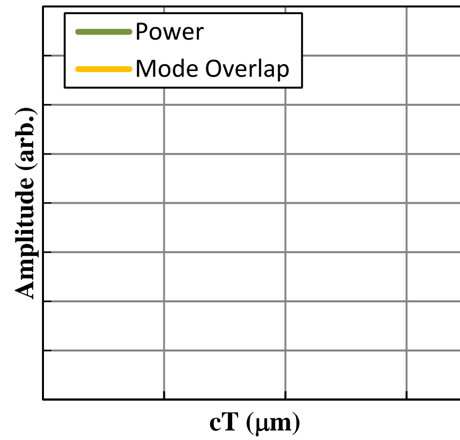

(c)

Figure 2.12 (a) Power monitors measuring input pulse power and transmitted pulses for three cases: no grating, open grating, and shorted grating. (b-c) Total power and mode overlap of the pulse exiting the (b) open grating and (c) shorted grating.

2.4 Potential for Photonic Integration

After reviewing the simulation results, we conclude that there is potential to use sub-wavelength metal gratings to create an integrated on-chip optical delay. For these simulations, we considered a very basic grating integration platform, but a more complicated semiconductor platform may be necessary to account for power loss via an active medium that supplies TM polarized gain. From the FEM and FDTD simulations, we know that the predicted group delay effect may only occur over a short range of integrated grating specifications and the delayed pulse may be distorted by radiation or substrate modes. In order to fully characterize the optical response of integrated sub-wavelength metal gratings, we must be able to measure gratings with varying periodicities and aspect ratios. Prior to this work there were no applicable demonstrations of fabricating high aspect ratio integrated metal grating on an InP-based platform. Chapter 3 will discuss the development of fabrication method for on-chip metal gratings.

2.5 Summary

In this chapter, we discussed the principle material properties that could make it advantageous to use patterned metals in photonic integrated circuits. While the range of applications is quite diverse, some design considerations remain fairly constant when it comes to exploiting the novel optical properties of metal gratings. Feature size must be much smaller than the desired wavelength of operation and TM mode

polarization is often required to achieve unique transmission properties. We focus on the potential impact of metal gratings on on-chip slow light applications and we utilize finite element method (FEM) and finite difference time domain (FDTD) simulation methods to predict the behavior of a metal grating integrated onto a simple InP-based waveguide platform. These simulation techniques lead us to conclude that it could be possible to measure a group velocity in light transmitted through an integrated metal grating that is designed properly. Moving forward, we then consider the future steps necessary to make on-chip photonic integration a reality.

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Chapter 3

Fabrication and Analysis of Metal Gratings

The fabrication of high aspect ratio structures on the sub-micron scale is a complicated challenge in itself. Achieving near-vertical sidewalls for deep etches combined with creating a robust structure that is not prone to structural breakage has been demonstrated on the micron scale in semiconductors, dielectrics, and metals [1]. However, creating high aspect ratio structures on the nanometer scale presents additional challenges. Conventional optical lithographic techniques are not sufficient for producing features on the order of 100nm. Additionally, integrating metals, dielectrics, and semiconductors into a single structure presents difficult processing conditions due to the widely varying etch chemistries of those materials[2].

Patterning metals on the nanometer scale is particularly challenging. Commonly used metals with high conductivities that are resistant to oxidation and degradation like gold and silver are very difficult to dry etch accurately without the use of specialized chemicals[3]. Metals that dry etch well like titanium or aluminum are subject to very fast oxidation and can break down quickly at the nanometer scale[4]. Figure 3.1 shows a previous attempt to dry etch gratings into aluminum. We can see significant undercut and rounding of the gratings despite much process development.

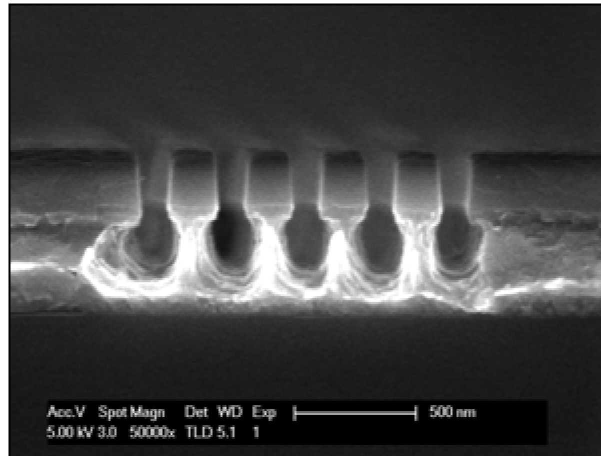


Figure 3.1 Example of chemical over etching in dry etched aluminum gratings.

The majority of processing done now with metals in semiconductor fabrication is via a liftoff process. But liftoff only works well with large geometries and there are often issues with metal detaching or inadvertently adhering to unwanted areas on the sample[5]. Because of these constraints on existing metal fabrication techniques, we determined that new, robust fabrication techniques need to be developed to create the metal grating structures desired.

3.1 Inverse Patterning Method Overview

The fabrication process developed for fabricating high aspect ratio nano-scale metal gratings is based on etching the negative or inverse of the metal grating pattern into a mulit-layer hardmask of SiO_2 and Chromium. After the hardmask is etched, the pattern can be transferred into a layer of thick dielectric or semiconductor based on the desired application. The spaces in the dielectric or semiconductor are then filled with metal to achieve the initial metal pattern. For example, to create a metal grating

with a period of 200nm and a duty cycle of 80 percent (metal lines are 80nm wide), the SiO_2 hardmask lines are defined to be 20nm wide and the 80nm opening will be filled with metal. This is a similar idea to the liftoff process but it eliminates many of the negative features of liftoff, such as rough sidewalls, large feature size, and low aspect ratio.

The inverse patterning method for fabricating metal gratings is very easily adapted to multiple material platforms. Here we will demonstrate how this method can be used to fabricate metal gratings on a thick SiO_2 cladding similar to one used for ultra-low-loss Si_3N_4 waveguides and SiO_2 cladding[6]. We begin with an InP substrate with a 500nm thick SiO_2 layer deposited via PECVD. This will be the grating layer that will be etched and the holes will later be filled in with metal. In order to be able to etch this layer more than 100nm, it will be topped with a 40nm thick layer of Chromium (Cr) deposited with electron beam deposition to act as a hardmask. In order to avoid resist features collapsing during lithography development as discussed above, the EBL resist used will be too thin to stand up to a long etch. The etch selectivity between Cr and SiO_2, as well as the selectivity from Cr to InP, is high, so Cr will act as good hardmask[7]. The Cr layer is coated with a final 40nm thick layer of SiO_2 deposited by PECVD. The final layer of SiO_2 is necessary because ebeam resist adheres poorly to Cr, resulting in unrepeatable lithography. The resist adheres very well to SiO_2, so it is chosen as the final layer of the material stack. The ebeam resist, ZEP520A:Anisol 2:1, is spun and the sample is ready for the inverse

patterning process to begin. The individual steps of the inverse patterning method are expanded on in the sections below.

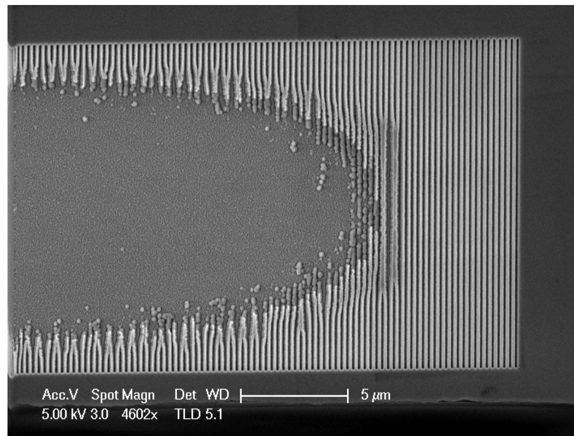
3.2 Fabrication

3.2.1 Electron Beam Lithography

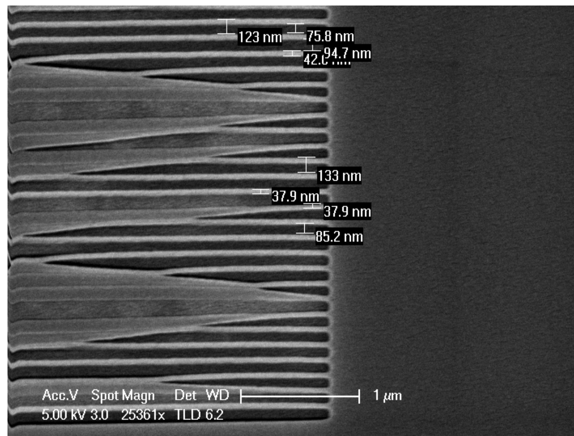
The necessity of using electron beam lithography (EBL) for nano-scale features fundamentally comes down to the fact that commercial optical lithography systems, particularly those available for use in the UCSB research cleanroom, simply cannot reliably produce the feature sizes necessary to make gratings designed for 1300nm communication systems. While holographic lithography can be a viable option for feature sizes on the 100nm scale, it is a very unreliable and unrepeatable process. The electron beam lithography tool available in the UCSB cleanroom, the JEOL model JBX-6300FS, is capable of creating single features as small as 7nm and reliably creating features on the order of 40nm. The JEOL ebeam writer can also reliably align patterns to within 100nm of the target position. Given the EBL tool specifications and the design flexibility it provides, electron beam lithography is an obvious choice for creating nano-scale gratings.

However, there are unique challenges that arise from EBL. Proximity effects can be a major problem when writing grating features. Exposing many lines very close together can cause the features in the middle of the pattern to be over-exposed and wash out when they are developed. Additionally, if the features written on the photoresist have a high aspect ratio, meaning that they are much narrower than the

thickness of the photoresist, the features will frequently fall over or collapse during photoresist development. Figure 3.2 shows an example of both proximity effects and collapsed resist.



(a)



(b)

Figure 3.2 (a) Example of EBL features washed out after developing due to proximity effects. (b) Example of high aspect ratio features that have collapsed after development.

There are many adjustable variables in EBL so finding solutions to the above challenges typically requires making changes to one or all of these easily changed variables: pattern geometry, exposure doses, and resist thickness. Through variable

adjustment and careful calibration, a repeatable process can be developed. Figure 3.3 shows developed gratings in ebeam resist that can be reliably and repeatedly written without proximity effects or resist collapse issues.

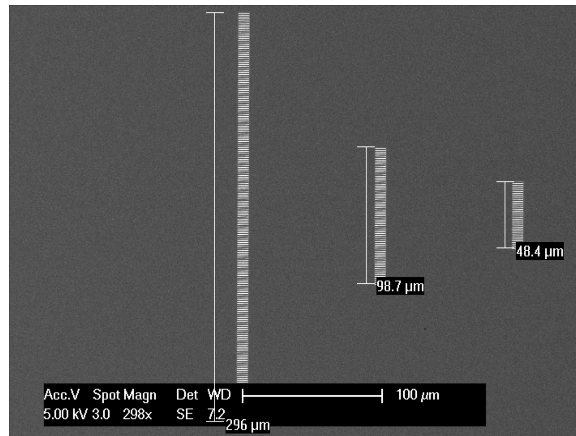


Figure 3.3 Gratings of variable length developed in ebeam resist without proximity effects or resist collapes issues.

Figure 3.4 shows a schematic of the EBL step in the inverse patterning process on the above described substrate, as well as a top down SEM image of gratings developed into ebeam resist.

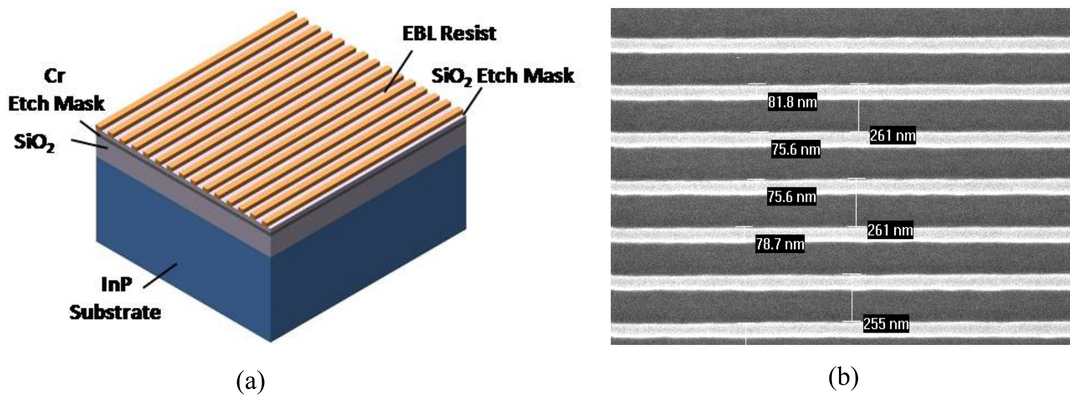
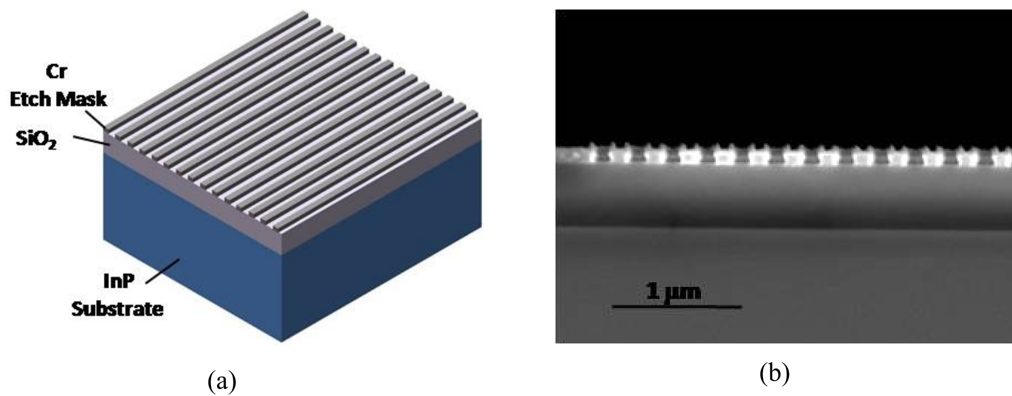


Figure 3.4 (a) Schematic of EBL on inverse pattern material stack. (b) Top down SEM image of gratings developed into ebeam resist.

3.2.2 Hardmask Etching

Due to the multi layer hardmask needed for the inverse patterning process, there are multiple etching steps necessary to create the grating pattern. After the ebeam resist has been developed, the top SiO_2 hardmask layer is etched with CHF_3 via reactive ion etching (RIE). Without removing the sample from the RIE chamber, a low power O_2 descum is run for no long than 5 minutes. A longer O_2 descum will lead to Cr oxidation and poorer etch selectivity in the next SiO_2 etch step. After the descum, the sample is removed and the ebeam resist is stripped.

After any resist remnants are removed from the sample, the Cr hardmask layer is etched via inductive coupled plasma (ICP) etching with a BCl_3/Cl_2 etch. Figure 3.5 shows a schematic of the hardmask etch step in the inverse patterning process on the above described substrate, as well as a cross-sectional SEM image of Cr gratings.



(a) (b)

Figure 3.5 (a) Schematic of Cr hardmask on inverse pattern material stack. (b) Cross-sectional SEM image of Cr gratings.

3.2.3 Dielectric or Semiconductor Deep Etching

After the Cr hardmask etch, the sample goes through one more etch. The length and chemistry of the etch depends on whether the material to be etched with the inverse grating pattern is dielectric or semiconductor. In this example, we are etching SiO_2 dielectric. For a deep SiO_2 dielectric grating etch, we use a CHF_3 based ICP etch. The ICP etch provides a more directional and physical etch than the RIE CHF_3 etch, which is more chemical. The ICP CHF_3 etch rate is also much faster.

Figure 3.6 shows a schematic of the SiO_2 dielectric etch step in the inverse patterning process on the above described substrate, as well as a cross-sectional SEM image of the SiO2 gratings. Note that the gratings shown undergo additional etching to reach the substrate.

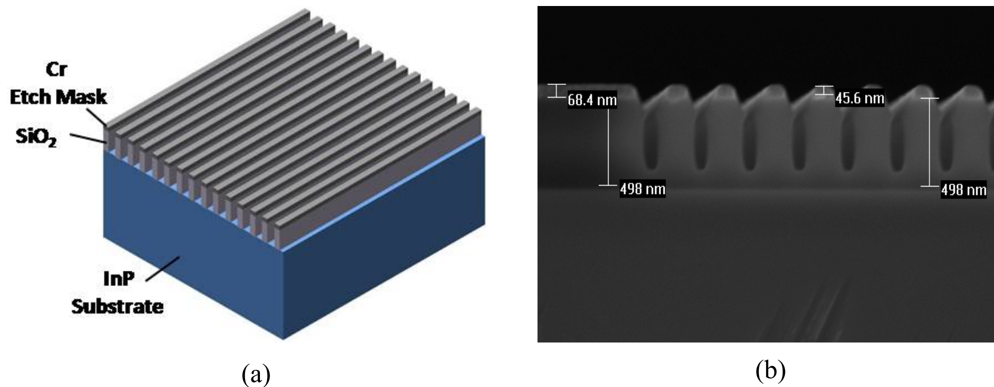
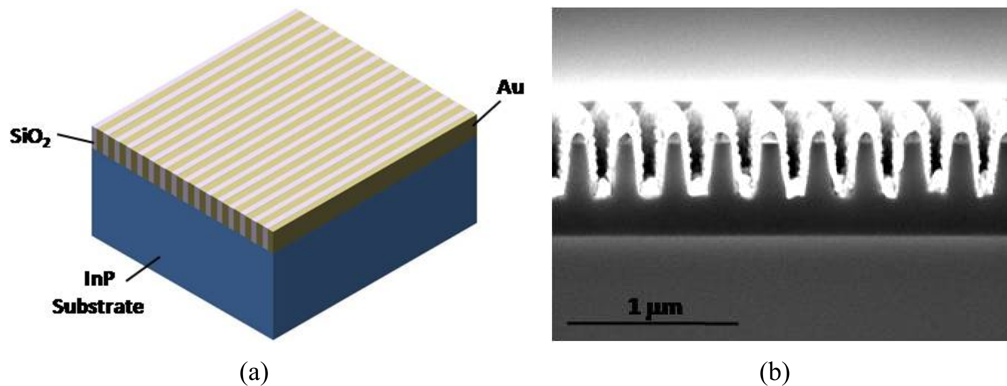


Figure 3.6 (a) Schematic of Cr hardmask with SiO2 deep grating etch on inverse pattern material stack. (b) Cross-sectional SEM image of SiO2 gratings.

At this point, the Cr hardmask can be removed using the same Cr etch used to pattern the Cr hardmask layer. Because of the excellent etch selectivity between Cr and SiO_2, very little damage occurs during the hardmask removal.

3.2.4 Metal Deposition and Liftoff

After the multi-layer hardmask etch and the final etch to transfer the inverse grating pattern, the sample is ready for metal deposition to complete the inverse patterning process of fabricating metal gratings. It is important use a metal deposition method that will completely fill in all of the gaps and coat the sidewalls of the gratings. Sputtering metals isn't commonly used in PIC applications, but it is the ideal for this application as the metal deposits in all directions. Figure 3.7 shows a schematic of the SiO_2 dielectric gratings with sputtered gold to complete the inverse patterning process, as well as a cross-sectional SEM image of the SiO_2 gratings. Note that the gratings shown did not undergo the additional etch to remove the Cr hardmask.



(a) (b)

Figure 3.7 (a) Schematic of the SiO2 deep grating etch with sputtered gold on inverse pattern material stack. (b) Cross-sectional SEM image of SiO2 gratings with sputtered gold.

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In order to fabricate metal gratings using the inverse patterning for photonic devices, it is not desired to coat the entire top of the sample with metal. For devices, it is necessary to incorporate an additional liftoff step before the metal deposition. Figure 3.8 shows Si_3N_4 waveguides fabricated with SiO_2 gratings patterned on top.

The dashed areas indicate where resist has been opened so that metal can be sputtered onto the gratings. The metal deposition is localized to the grating areas and will be lifted off the majority of the sample.

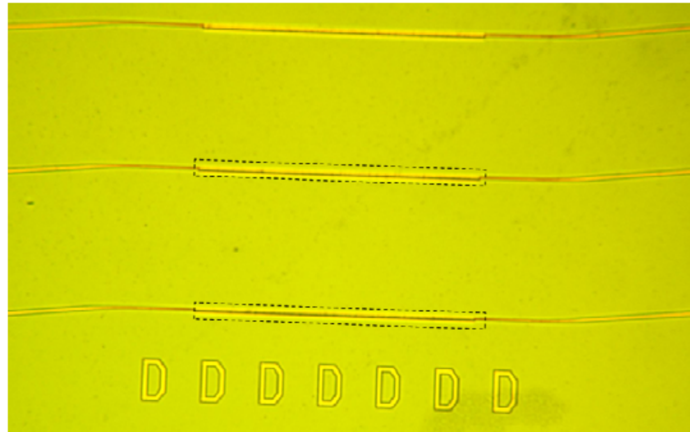
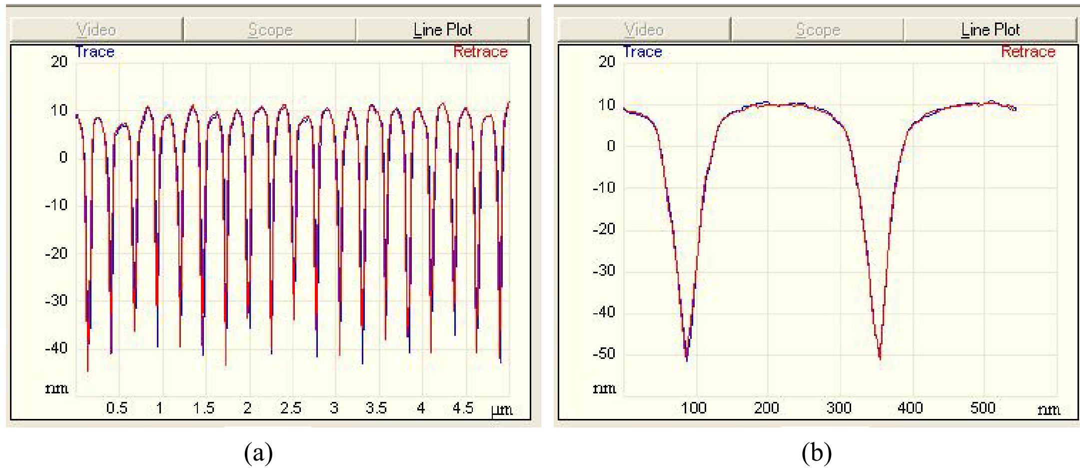


Figure 3.8 Si_3N_4 waveguides fabricated with SiO_2 gratings patterned on top Dashed line indicates areas where resist has been opened so metal deposition can be localized to gratings.

3.3 Grating Characterization

In order to verify that the metal gratings were fabricated according to our specifications, we used two additional verification techniques to show that we were in fact achieving the grating pitch that we desired. We fabricated two samples with grating pitches of 256 nm and 264 nm respectively. Atomic Force Microscopy (AFM) was used to measure the grating pitch after the initial EBL and again after the final SiO_2 deep grating etch. Figure 3.9 shows AFM line plots of the gratings measured. Because the AFM tip used will only measure depths of approximately 150nm, the bottoms of the gratings are not seen. Cross-sectional measurements are the most

accurate method for measuring depth, but they do irreparable damage to the sample. AFM provides a good first measurement to ensure the gratings are fabricated to specification.



(a) (b)

Figure 3.9 (a) AFM line plot of many etched grating periods. (b) Zoomed-in AFM plot to more accurately measure grating period after etch.

After the AFM measurement, we performed a grating diffraction experiment using a 325nm wavelength UV laser after the final etching fabrication step[8]. Figure 3.10 shows that in both cases the grating period was measured to be 2nm or less within our target period. This margin of error is to be expected in the cases of these measurement techniques. Both AFM and grating diffraction measurements require the experimenter to use best judgment measurement techniques rather than digital, computerized measurements. EBL is widely accepted to be a very accurate lithography technique, so without optical spectral analysis, the initial characterizations indicate that the fabrication is within specification.

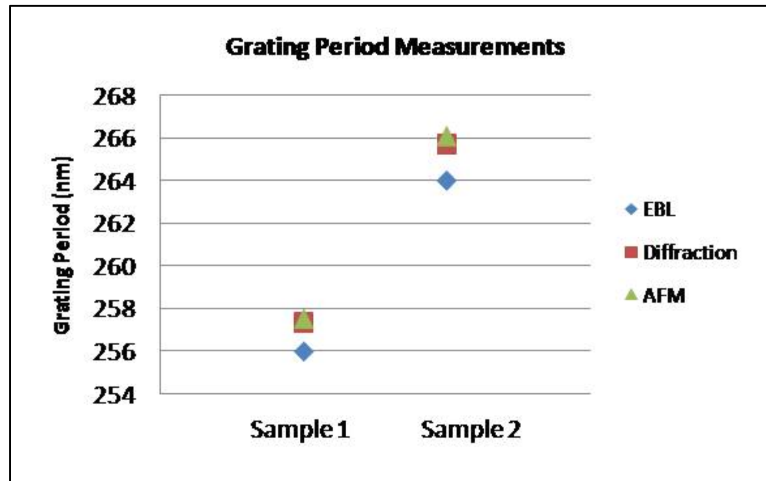


Figure 3.10 Plot of EBL, grating diffraction, and AFM measurements of grating pitch.

After we verified that we had an accurate and reliable method for fabricating metal gratings, we used the previously cited ultra-low-loss Si_3N_4 waveguide platform to take preliminary measurements of optical modes as they passed through the grating. Figure 3.11 shows a schematic of the overview of the fabrication process of metal gratings integrated with waveguides on the ultra low loss platform.

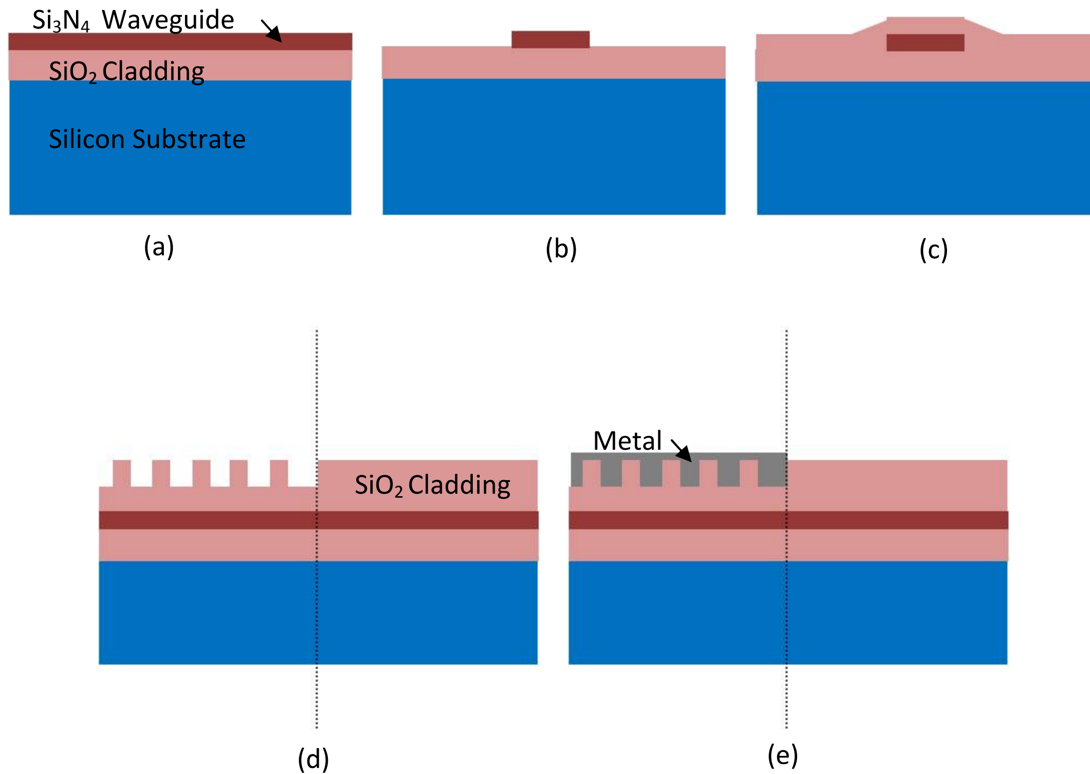
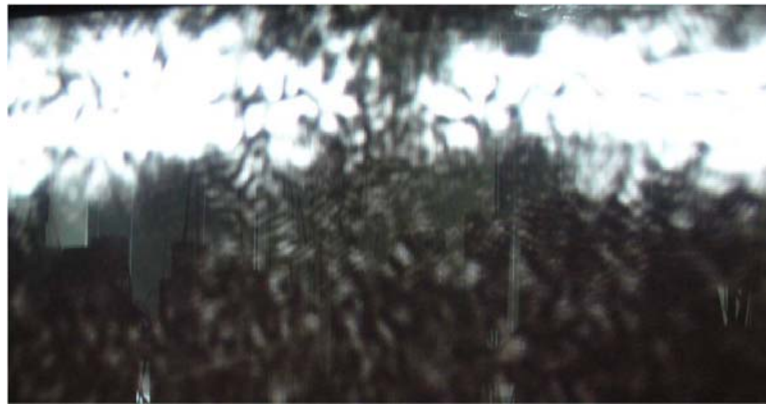


Figure 3.11 (a-c) Cross-section showing the Si3N4 waveguide layer patterned with optical lithography, etched with ICP, and deposited with SiO2 upper cladding (d-e) Cross-section showing the grating etch and metal deposition.

After the fabrication was complete, the gratings integrated with waveguides were diced out and polished. Light was coupled in via optical fiber and measured with an off chip detector. The measured slow light effects were very negligible, but we did see interesting results by viewing cross-sections of modes with an IR camera. Figure 3.12 (a) shows the captured image from the IR camera when light was passed through a 5um long grating and (b) shows the IR image when light was passed through a 50um long grating.

(a)



(b)

Figure 3.11 (a) RF camera view of optical waveguide mode after passing through 5um long metal grating. (b) RF camera view of optical waveguide mode after passing through 50 um long metal grating.

We can visibly see that the 50um grating is reflecting a much more significant portion of the optical mode. While it does appear that a good portion of the light in Figure 3.11 (b) is being scattered compared to (a), it should be noted that the ultra-low-loss Si_3N_4 waveguides have a very low confinement factor. After measuring negligible amounts of the effect we intended to measure and seeing these IR images,

we decided to focus on the more feasible and near-term possibility of using metal gratings for mirrors. The following chapters chronicle the results of that study.

3.4 Summary

This chapter discussed the challenges associated with fabricating sub-wavelength scale metal gratings that can be integrated with a wide variety of material platforms. We present a fabrication approach that we call the inverse patterning method. The inverse of the desired grating pattern is etched into a semiconductor or dielectric through the steps of electron beam lithography, multi-layer hardmask etching, and a deep grating etch. Then metal is sputtered into the inverse grating creating the initially desired metal pattern. Liftoff techniques can be used to remove any excess metal from the sample. The inverse pattering method was verified as an accurate fabrication technique through AFM measurement and a grating diffraction experiment. After experimenting with optical transmission through the metal gratings on an ultra-low-loss Si3N4 waveguide platform, we determined that metal gratings possessed potential as compact, integrable mirrors for photonic integrated circuits.

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Chapter 4

Photonic Device Integration

In the previous chapter, we determined that a more realistic near-term integration application for sub-wavelength metal gratings was to use them as mirrors for in-plane lasers. Here we present our design and integration strategy based on previous work done at UCSB and the design requirements of many integrated patterned metal structures, namely nano-fabrication potential and TM mode support.

4.1 Integration Strategy

Monolithic integration of photonic devices on InP-based materials platforms has become a specialty at UCSB. Device architectures and fabrication processes for lasers, modulators, detectors, wavelength converters, and more have been robustly developed[1]. While attempting to integrate sub-wavelength metal gratings as DBR laser mirrors certainly requires some process modifications to the standard InP PIC processes developed in the past, we do not wish to abandon the collective knowledge of the last decade of photonic integrated circuit designers at UCSB. In fact, it is this comprehensive knowledge base that allows novel integration to occur in the time frame of a Ph.D. project. We will used the standard InP PIC process developed in the Blumenthal group[2] as a starting point and make modifications only as necessary.

Aside from the newly developed metal grating fabrication process discussed in Chapter 3, the most notable deviation is moving from the standard compressively strained InGaAsP offset QW platform to a TM gain medium. In the next section, we discuss the material parameters of the active medium chosen and justification for selecting it.

4.2 Material Platform

As discussed in Chapter 2, a material platform that supports TM gain is critical for many plasmonic and metamaterial applications of patterned metal gratings. As we shift of our focus from on-chip slow light elements to DBR lasers with metal grating mirrors, we want to maintain focus on high impact areas of integration for these structures. For this reason, we chose to fabricate our lasers on an active offset QW platform that supplies gain to the TM mode. After comparing various TM gain mediums including different quantum well structures and bulk active material, we determined that high gain and low threshold current densities provided from AlInGaAs QWs would best suit our application[3]. The reported material parameters obtained from broad area lasers are an internal efficiency of 0.7 W/A, internal loss of 16 cm^{-1}, threshold current density of 100A/cm^2 per quantum well, and gain parameter, g_0 of 90cm^{-1}[4]. While we would like to maximize the amount of gain possible, we chose to limit the number of wells and barriers to seven and eight, respectively, because of the heavy strain of the quantum wells. We have also designed the material platform around a lasing wavelength of 1300nm. Again, this

choice is made to try to minimize the amount of strain in the QWs, as a 1550nm gain profile would require further tensile straining of the QWs Table 4.1 shows the base epitaxial layer structure of AlInGaAs QW structure selected.

Table 4.1 Base epitaxial layer structure for tensile strained AlInGaAs QWs

Layer	x	y	Perpendicular Strain (%)	Thickness (A)	Doping
p-InP buffer	---	---	0	4000	(p) 1E18
1.10 Q $In_xGa_{1-x}As_yP_{1-y}$ Stop Etch	0.8550	0.3180	0	150	(p) 1E18
p-InP buffer	---	---	0	1500	(p) 1E18
InP Setback	---	---	0	500	UID
$In_xGa_{1-x}As_yP_{1-y}$ SCH	0.8600	0.3200	0.047	400	UID
$Al_xGa_yIn_{1-x-y}As$ barrier	0.3000	0.0800	0.64%	200	UID
$Al_xGa_yIn_{1-x-y}As$ well x7	0.0640	0.6410	-1.65%	100	UID
$Al_xGa_yIn_{1-x-y}As$ barrier x7	0.3000	0.0800	0.64%	200	UID
$In_xGa_{1-x}As_yP_{1-y}$ SCH	0.8600	0.3200	0.047	400	UID
InP Stop Etch	---	---	0	150	(n) 3E16
1.10 Q Waveguide - $In_xGa_{1-x}As_yP_{1-y}$	0.8550	0.3180	0	3200	(n) 3E17
n-InP buffer	---	---	0	500	(n) 4E17
n-InP buffer	---	---	0	500	(n) 7E17
n-InP buffer	---	---	0	19000	(n)1E18
n-type InP substrate	---	---	0		(n)>5E18

Since we have chosen an offset quantum well platform, the final material stack for the fabricated devices will require a p-doped InP cladding regrowth and a heavily p-doped InGaAs contact layer. The regrowth is crucial to lowering waveguide losses in the devices as well as providing low resistance electrical contacts. Figure 4.1 shows a schematic of the fully regrown epitaxial layer structure including growth specifications.

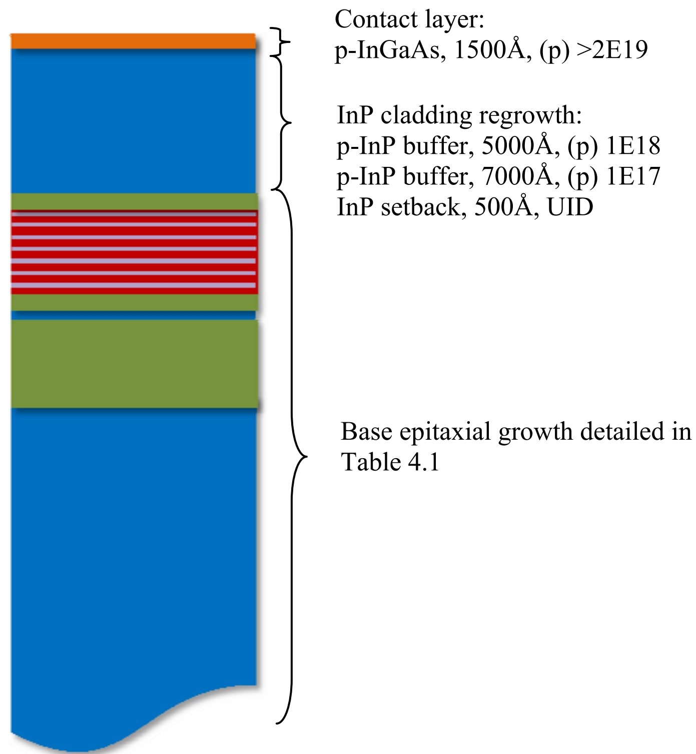

Figure 4.1 Schematic of regrown epi material

One additional feature of this regrown offset quantum well platform is that we have chosen a 1.2 micron thick p-InP buffer layer as compared to the standard UCSB offset QW platform which uses a 2.0 micron thick buffer layer. This choice was made so that it would be easier to fabricate the metal gratings closer to the waveguide and QW layers, where the majority of the optical mode is confined. A thicker buffer layer may reduce waveguide losses slightly, but it may prove prohibitive to have to etch the gratings more than 1 micron deep. Further discussion of the grating design process can be found in Section 4.3.

Figure 4.2 shows the energy band diagram of the complete epitaxial layer structure. The quantum well transitions are drawn as the light hole band, which provides TM gain. Some TE gain will be supplied through the heavy hole band, but for heavily tensile strained materials such as ours, the TE gain will be minimal[5].

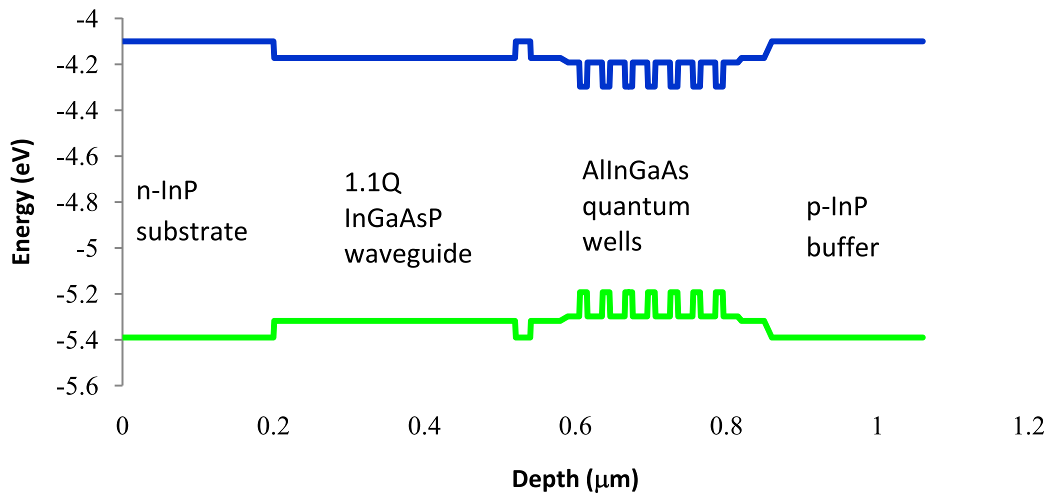

Figure 4.2 Energy band diagram of regrown offset quantum well material platform

A secondary mass ion spectroscopy (SIMS) measurement was performed on the regrown material in order to see the doping levels in the regrown material and at the regrowth junction. There have been issues in the past with Zinc (Zn) doping levels being too high and bleeding over into the undoped junction. There have also been issues of a spike in Silicon (Si) contaminants at the regrowth interface, which can severely impair current transport across the junction[1]. Figure 4.3 shows a SIMS measurement of a preliminary regrowth designed to avoid both Zn and Si contamination. We can see from this measurement that the Silicon contamination was mitigated, but the Zn levels were over corrected and were now too low. This would

not necessarily been catastrophic for device performance, but may have caused inefficient current injection. The doping issue was later corrected with an additional round of regrowth to increase the doping and complete the junction.

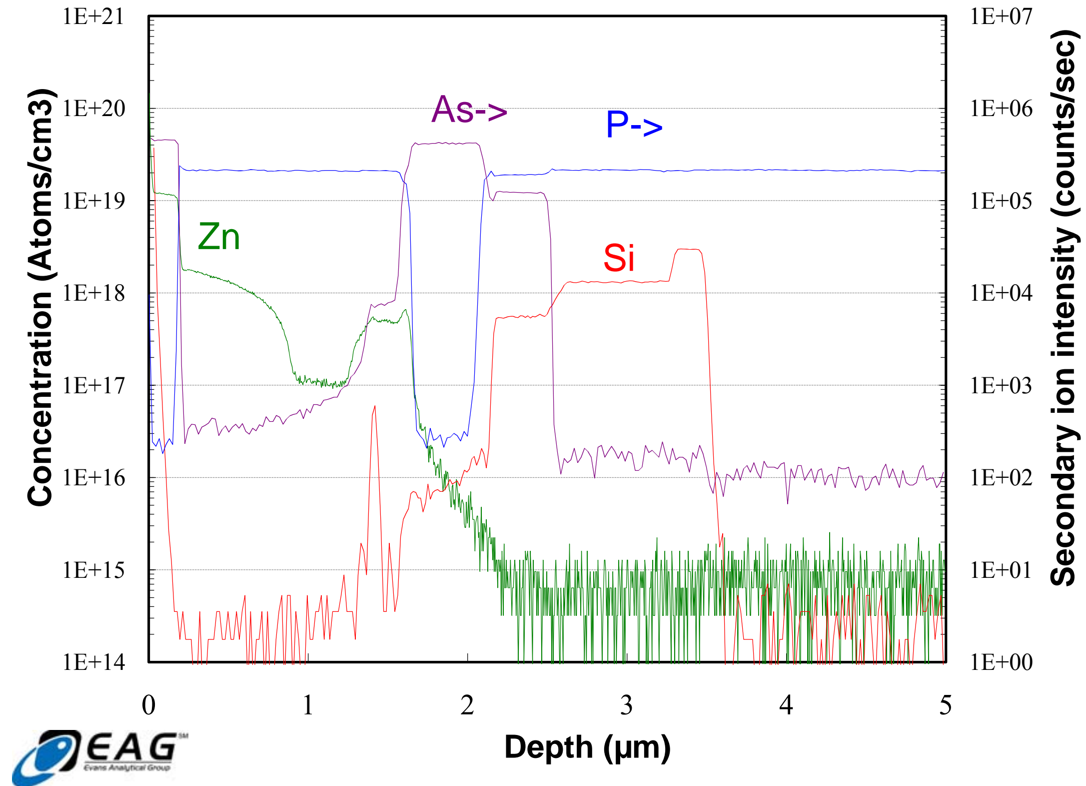

Figure 4.3 Preliminary SIMS measurement of epitaxial doping showing low Zn doping that was later corrected in subsequent regrowths.

After the issues with material regrowth were corrected, we were able to measure the bulk material properties by fabricating broad area lasers. The lasers were 50 um wide and cleaved to three different lengths. Figure 4.4 shows the results of the broad area laser testing.

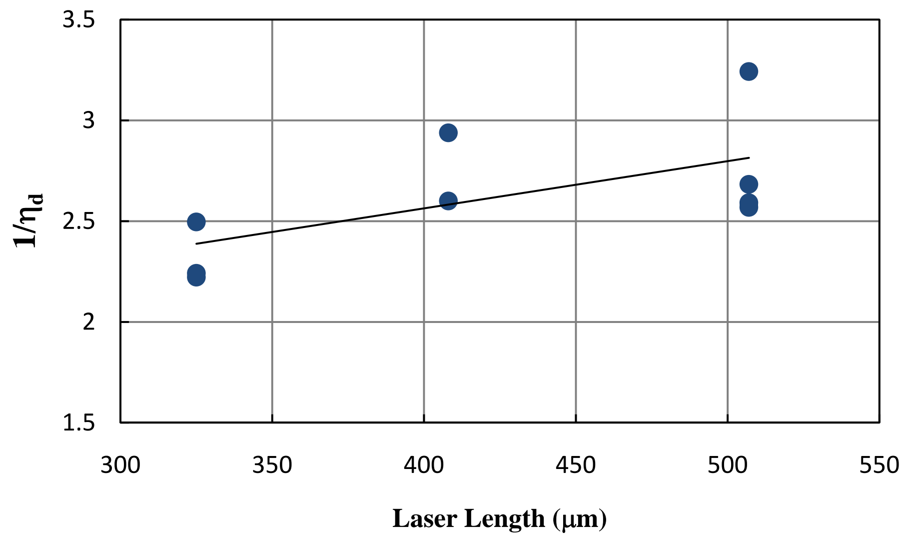

Figure 4.4 Broad area laser tasting results yield a measured material loss of 16.41 cm^{-1} and an injection efficiency of 61.48%.

The plot of broad area laser performance allows us to calculate a material loss, α_i, of 16.41 cm^{-1}. The measured material loss is within a reasonable range and is very close to that reported by those that first developed the material platform. Some lasers fabricated at UCSB have been measured to have around 90% injection efficiency, but the injection efficiency of these lasers was subpar at 61.48%. Low injection efficiency could later effect device performance and heating, even causing the junction to break down at high current values[6]. However, given that we have corrected issues with the material doping and we have measured reasonable material loss values, this material meets the necessary design requirements and is suitable for the application of in-plane lasers with metal mirrors.

4.3 Waveguide Design

Waveguides are a crucial part of fabricating in-plane lasers because they define the active laser cavity and guide light out of the laser to be used by other devices in the integrated circuit. The waveguide design chosen is a surface ridge design that is commonly used in PICs at UCSB. This waveguide design is very versatile in that it is multimode and supports both TE and TM polarizations. The regrown surface ridge design also lowers the waveguide loss. This design has been used for large scale PICs with integrated lasers and has proven to be very robust, both in device performance and fabrication tolerance. The waveguide is designed to be 3 microns wide and with the same depth as the InP cladding regrowth, in this case 1.2 microns. Figure 4.5(a) shows a cross-section of the active waveguide that will be used for the laser cavity and other active circuit elements along with the active optical mode profile. Figure 4.5(b) shows a cross-section of the passive waveguide that will be used guide the light in-plane around the chip and the passive optical mode profile. The effective indices of the active and passive waveguide are 3.41 and 3.24, respectively.

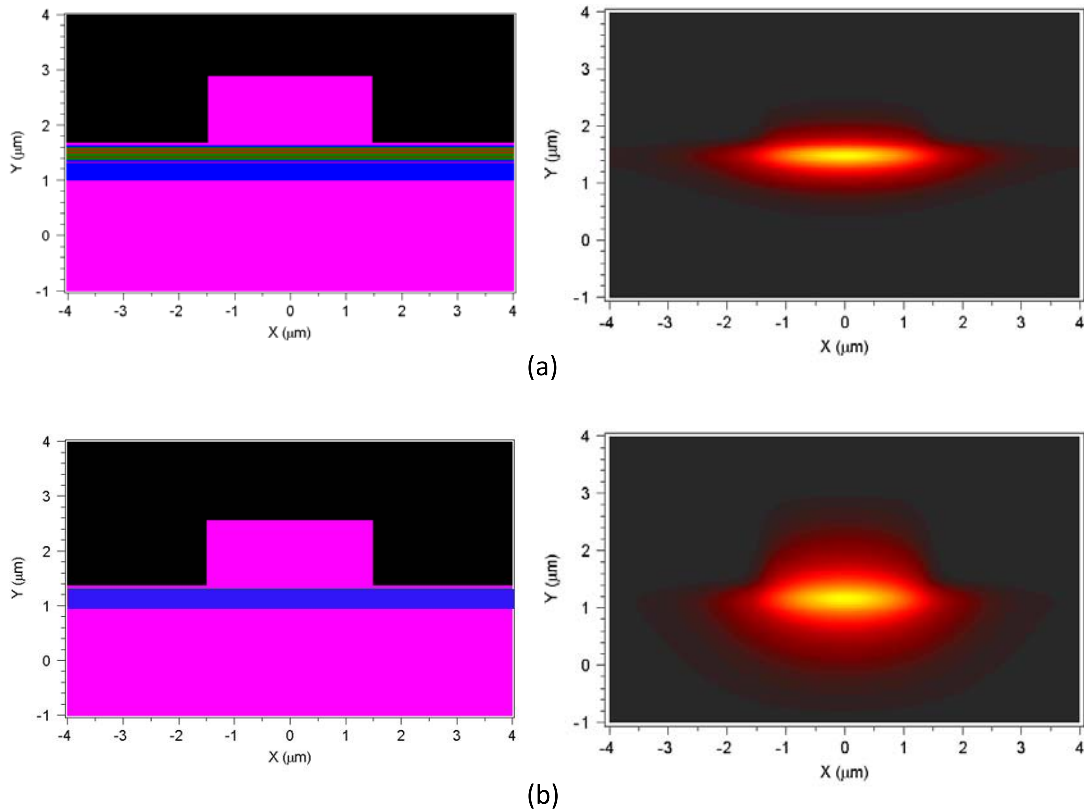

Figure 4.5 (a) Active waveguide cross-section and mode profile. (b) Passive waveguide cross-section and mode-profile.

In order to demonstrate lasing in the active waveguide cavity, we tested the cleaved active waveguide structures for Fabry-Perot lasing. The CW lasing spectrum of a 510 µm cavity Fabry-Perot cooled to 15 °C is shown in Figure 4.6. The shape of the lasing spectrum looks as expected with a mode spacing of 0.44 nm. This corresponds to an active group index, n_{ga}, of 3.94[7]. The center peak lasing wavelength, 1330nm, is longer than expected, leading us to believe that these devices may be heat sensitive and heating may factor in to the grating lasers CW and pulsed performance.

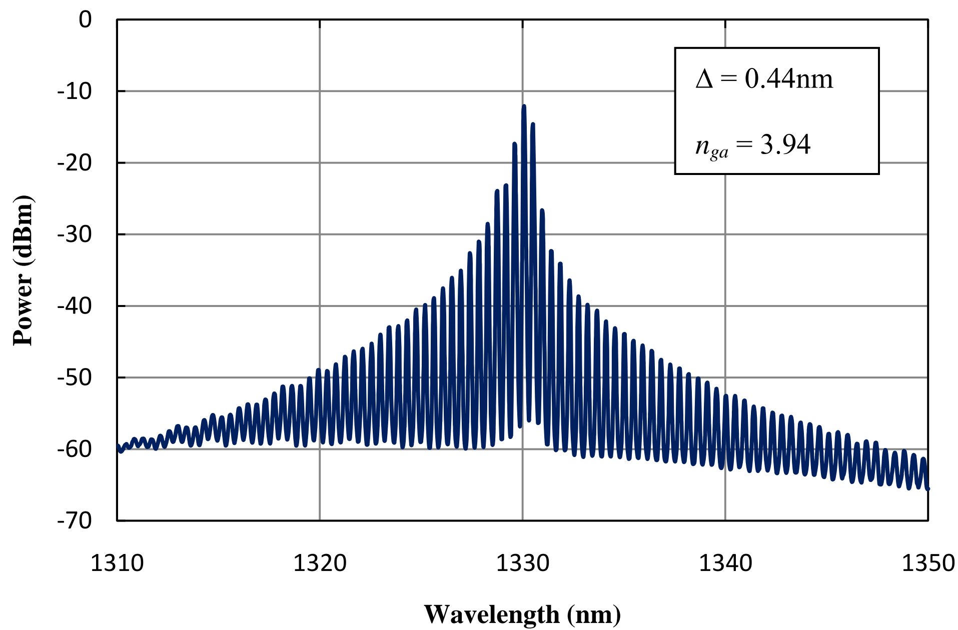

Figure 4.6 Fabry-Perot lasing spectrum of 510um cleave laser cavity.

Many successful PICs have been developed using the previously described waveguide design and it has again been demonstrated as a viable integration tool with our AlInGaAs material platform. The next step is to design the gratings that will define the cavity and wavelength selectivity of the lasers.

4.4 Mirror Design

In order to fully characterize metal gratings as integrable optical elements, we will incorporate both metal and standard semiconductor regrown mirrors into our laser design. The following sections will show the design methodology we used for each grating.

4.4.1 Semiconductor Grating Mirror Design

The use of semiconductor regrown gratings as mirrors for in-plane lasers like distributed Bragg reflector (DBR) and distributed feedback (DFB) lasers have been extensively used and well documented for a wide variety of semiconductor material platforms[8]. For offset quantum well platforms, the gratings are patterned and etched into the waveguide layer before the cladding regrowth. Once, the material has been regrown, the waveguide and grating cavity is defined in the cladding over the gratings. Because this theory has been so well reported, we will not elaborate extensively on it here, but we will discuss the fundamental design elements.

For our material platform and waveguide architecture, we determine that the periodicity of the semiconductor gratings will range from 199nm-202nm for Bragg wavelengths of 1280nm-1310nm. The periodicities are found using equation 4.1.

$$\Lambda = \frac{\lambda_B}{2 \cdot n_{eff}} \tag{4.1}$$

Once we have determined the grating indices, we can calculate the reflectivity of a single grating period, and subsequently the reflectivity of the grating with respect to length[8], as seen in Figure 4.7. This relationship of reflectivity vs. length can be use to find the coupling coefficient of the grating, kappa. For a semiconductor grating that is etched 60nm in to the waveguide, we expect a kappa value of ~ 400 cm^{-1}.

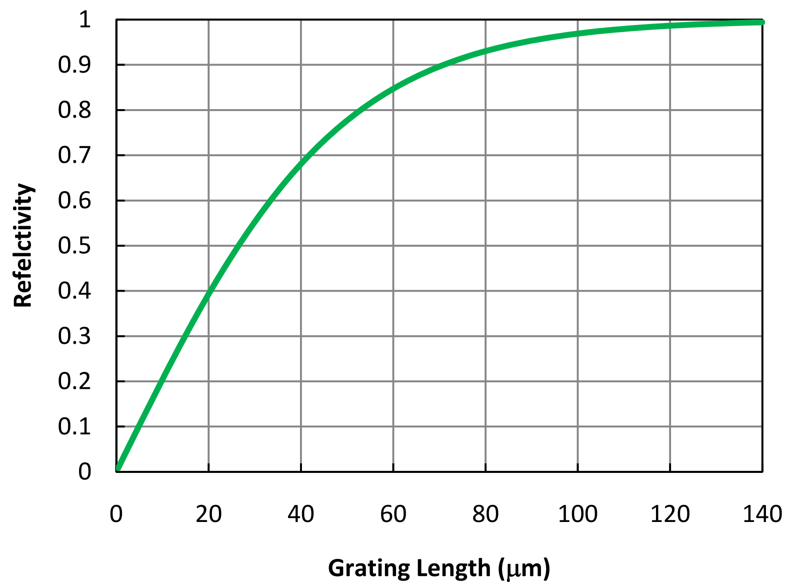

Figure 4.7 Regrown semiconductor grating reflectivity vs. grating length

We are interested in semiconductor gratings as a comparison tool for characterizing metal gratings. Next we'll turn our attention to the metal grating design.

4.3.2 Metal Grating Mirror Design

In Chapter 3, we discussed the metal grating fabrication process. Since our grating will be integrated from the top of the waveguide, etch depth will play a crucial role in determining the reflectivity of the grating. Because the grating sits far away from the waveguide, the individual grating reflections can be very small. Figure 4.8 shows how grating reflectivity varies based on the grating length for many different etch depths. We can see that for shallow etch depths, even a very long grating will not have a strong reflectivity.

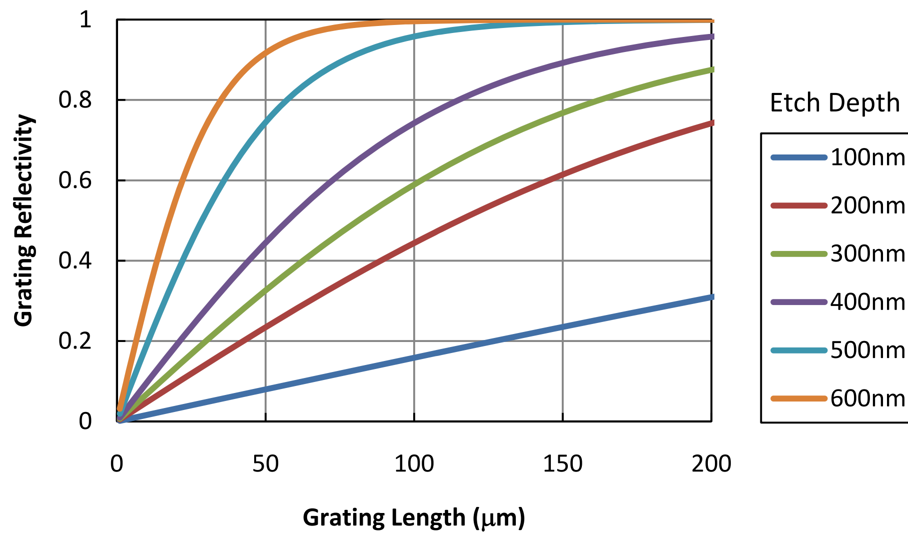

Figure 4.8 Metal grating reflectivity vs. grating length for various etch depths.

As the grating reflectivity vs. length increases for deeper grating etch depths, so does grating coupling coefficient, kappa. Figure 4.9 shows a plot of kappa values for increasing grating etch depths. This plot allows us to see how crucial etch depth is to grating coupling in our device, as the coupling begins to go up exponential as the grating gets closer to the waveguide. Strong grating coupling is necessary to achieve high mirror reflectivites in a small amount of space, as we would like to do, so it will be important for us have a well-calibrated grating etch to reach our desired depth. A small digression from the design will result in a big change in the grating coupling.

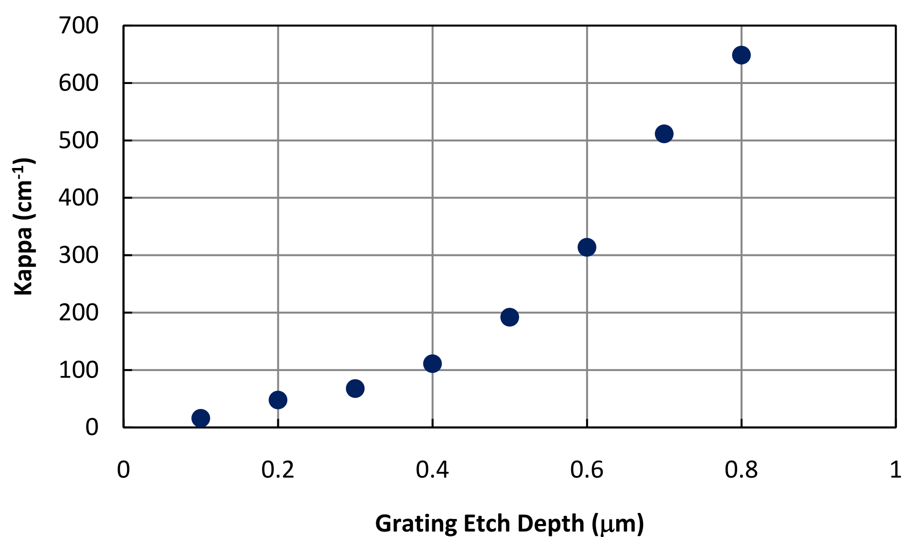

Figure 4.9 Grating coupling coefficient vs. grating etch depth for simulated metal grating parameters

It is also important to consider the frequency selectivity of the gratings as well as their reflectivity. In some cases, one many want to design a grating with a fairly flat mirror loss spectrum so that the laser could be easily tuned. Or in other cases, it may be important to have a very narrow mirror loss spectrum so that single frequency data can be transmitted over long distances. For our application, we would like to demonstrate single frequency lasing, so we will make sure to include some gratings that are very frequency selective. Figure 4.10 shows the mirror loss vs. wavelength of a metal grating mirror of various lengths. All the of the mirror lengths have the same kappa, as they would in a single processing run, and we can see that the wavelength selectivity of the grating can be controlled by the grating length.

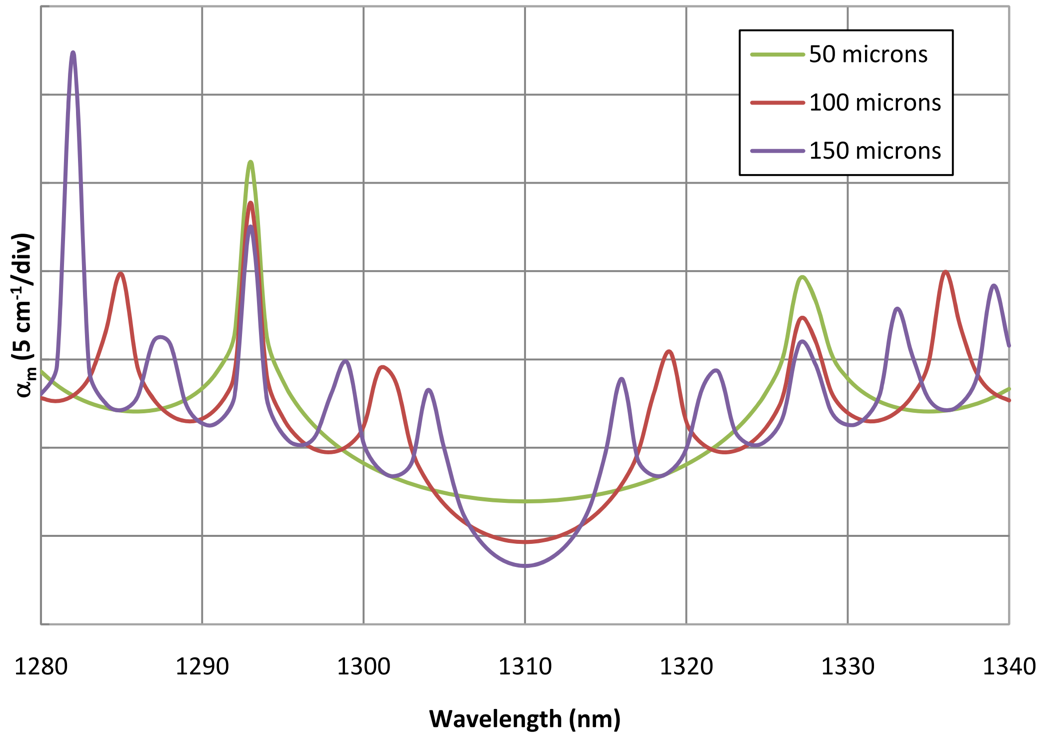

Figure 4.10 Mirror loss vs. wavelength for various metal grating lengths.

Now that we have a better understanding of the design space that metal gratings integrated with surface ridge waveguides occupy and their potential as laser mirrors, we can lay out a device split chart to fabricate, test, and characterize the gratings.

4.5 Device Layout

With a large device split chart, it is important to layout devices in a way that can be easily fabricated and tested. We needed a device layout that would allow for integrated device screening with on-chip detectors as well as the ability to cleave out

devices with facets perpendicular to the outgoing incident light. Figure 4.11 shows our device layout with alternating columns of lasers and detectors all connected with a continuous waveguide.

We will fabricate and test two types of DBR laser. The first is seen in column E of Figure 4.11, DBR lasers with two metal grating mirrors. Both mirrors will have the same Bragg wavelength, but the mirror lengths will be asymmetrical. The intention with this design choice is to be able to compare the light measured out of both sides of the laser and extract the reflectivity values. The second type of DBR laser, as seen in column D of Figure 4.11, will have one metal grating mirror and one semiconductor mirror. We will design both mirrors to have the same Bragg wavelength, but the periodicity of the mirrors will be different because of the different effective indices. Again the front and back mirrors will be different lengths in order to compare the reflectivities of the regrown semiconductor and metal grating mirrors.

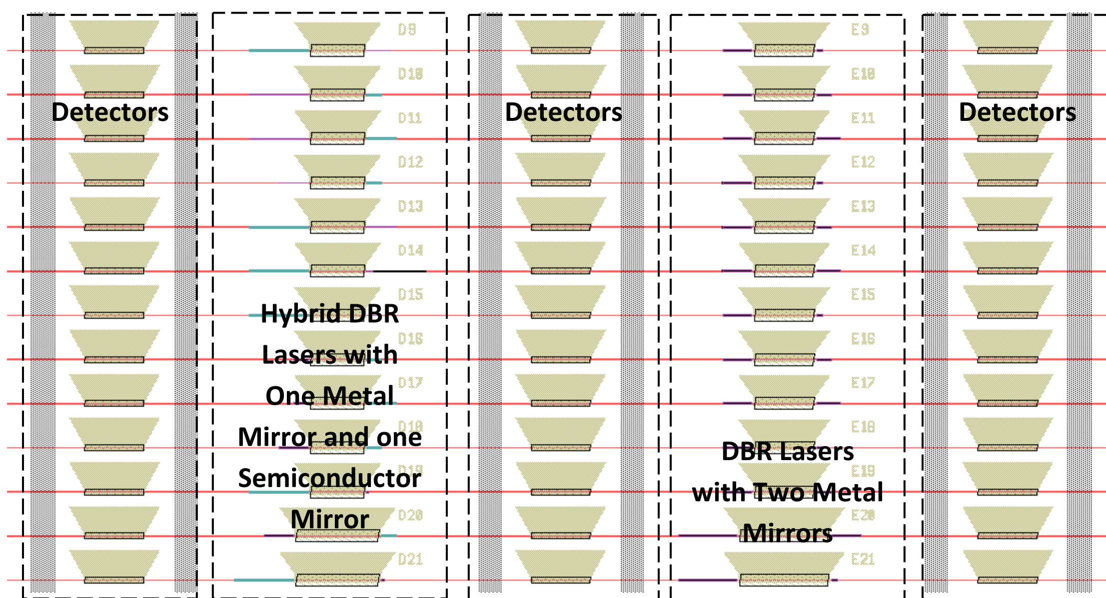

Figure 4.11 Device layout with alternating on-chip detectors and lasers separated by cleave spaces.

4.6 Summary

Incorporating the nearly universal design considerations we found to be true for sub-wavelength metal structures, we design distributed Bragg reflector lasers to demonstrate the potential for photonic circuit integration. An InP-based material platform is chosen along with highly tensile strained AlInGaAs QWs to provide TM gain. We use basic in-plane laser design concepts to design DBR lasers with a wide variation of parameters. Grating pitch, mirror length, cavity length, and mirror material are all varied to provide optimal opportunity for proof of concept. The resulting devices are laid out with the option to use on-chip detectors or to cleave out the lasers and measure light off chip.

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Chapter 5

Device Fabrication

Developing a device fabrication process for new structures on a previously unused material platform with few previously reported experimental results is a very time intensive process. While collective intelligence and literature can be very valuable tools as we make an initial processing plan, there are frequently unexpected processing results that require additional process development effort. In the case of these devices, there is very robust knowledge of InP-based materials processing[1], as well as, significant work with AlInGaAs quantum wells bonded to silicon substrates[2], but there were significant parts of the process that were unknown and needed to be developed. Two particularly challenging aspects of the fabrication that will be highlighted are regrowing InP over AlInGaAs wells and fabricating nano-scale grating on microscale waveguides. We present here our processing approach to integrating sub-wavelength scale metal gratings onto an InP-based materials platform with heavily tensile-strained AlInGaAs quantum wells.

5.1 Device Fabrication Overview

All processing for these devices was done on quarter 2" wafers. The fabrication process consists of two electron beam lithography (EBL) steps and between five and seven optical lithography steps depending on if deeply etched waveguide are required. Table 5.1 summarizes the key processing steps. Many of these processing steps have been detailed in previous work[3] or in earlier chapters of this thesis so we will mainly focus on new process development or how the standard processes were adapted to this platform.

In addition to the summarized process flow presented in Table 5.1, Figure 5.1 shows a schematic of topographical changes that occur on the sample for major processing steps. Figure 5.1(a), (d), and (f) are cross-sectional views in the yz-plane, perpendicular to the waveguides. This view shows the active and passive waveguide structures as well as the direct vias and contacts on the waveguides. Figure 5.1(b), (c), and (e) are cross-sectional views in the xz-plane, parallel to the waveguides. This vantage point shows the grating development steps that are etched perpendicular to the waveguide.

The majority of the time-intensive and critical steps in the process were related to fabricating the metal gratings, so an effort was made to keep the micro-scale processing straight-forward. Although early steps in the fabrication proved not to be trivial, we built as much robustness into the fabrication process as possible. The devices were laid out to provide generous lithography tolerances of up to 1 μm tolerance in the y direction and up to 5 μm of lithography tolerance in the x direction.

The following sections provide detail of the development of individual process steps.

Table 5.1 Summarized process flow for device development

Processing Step	Purpose	Equipment Used
Active/passive definition	Define active regions and remove QW material from all other areas	PECVD + RIE#2($CH_4/H_2/Ar$)
Active passive wet etch	Finish active passive etch and clean up stray material	Wet etch ($H_3PO_4:H_20_2:H_20$ 1:5:15 + $H_2SO_4:H_2O_2:H_20$ 1:1:10)
Semiconductor gratings	Etch grating for semiconductor regrown mirrors	PECVD + EBL + RIE #3(CHF_3) + RIE#2($CH_4/H_2/Ar$)
Cladding regrowth	Regrow p-type InP cladding and InGaAs contat layer	Out of house
Grating definition for metal gratings	Deposit multi-layer hardmask and define inverse pattern of metal gratings	PECVD + Ebeam#1 (Cr) + PECVD + EBL
Grating etch for metal gratings	Deeply Etch inverse pattern of metal gratings into InP cladding	RIE#3 (CHF_3) + ICP (BCl_3/Cl_2) + ICP (CF_4)+ ICP (BCl_3/Cl_2)+ RIE#2 ($CH_4/H_2/Ar$)
Ridge waveguide definition	Etch surface ridge waveguides	PECVD + RIE#2($CH_4/H_2/Ar$)
Wet etch protection	Protect deeply etch regions and cleanup waveguide etch	Wet etch (3:1 H_3PO_4:HCl)
Deep ridge definition	Dry etch deep ridge regions	Ebeam#1 (Cr) + RIE#2($CH_4/H_2/Ar$)
Metal deposition for metal gratings	Sputter metal into deeply etched InP gratings	Sputter #4 (Au)
Direct Via	Open vias on areas for contact metal	PECVD + RIE#3(CH_4/O_2)
P-metal deposition	Deposit Ti/Pt/Au contacts	Ebeam#4
Lapping	Thin sample for cleaving and carrier transport	Manual lapping tool
N-metal	Deposit Ti/Pt/Au backside contacts	Ebeam#4
Device cleaving and mounting	Cleave facets, separate devices, and prepare for testing	Loomis cleave tool

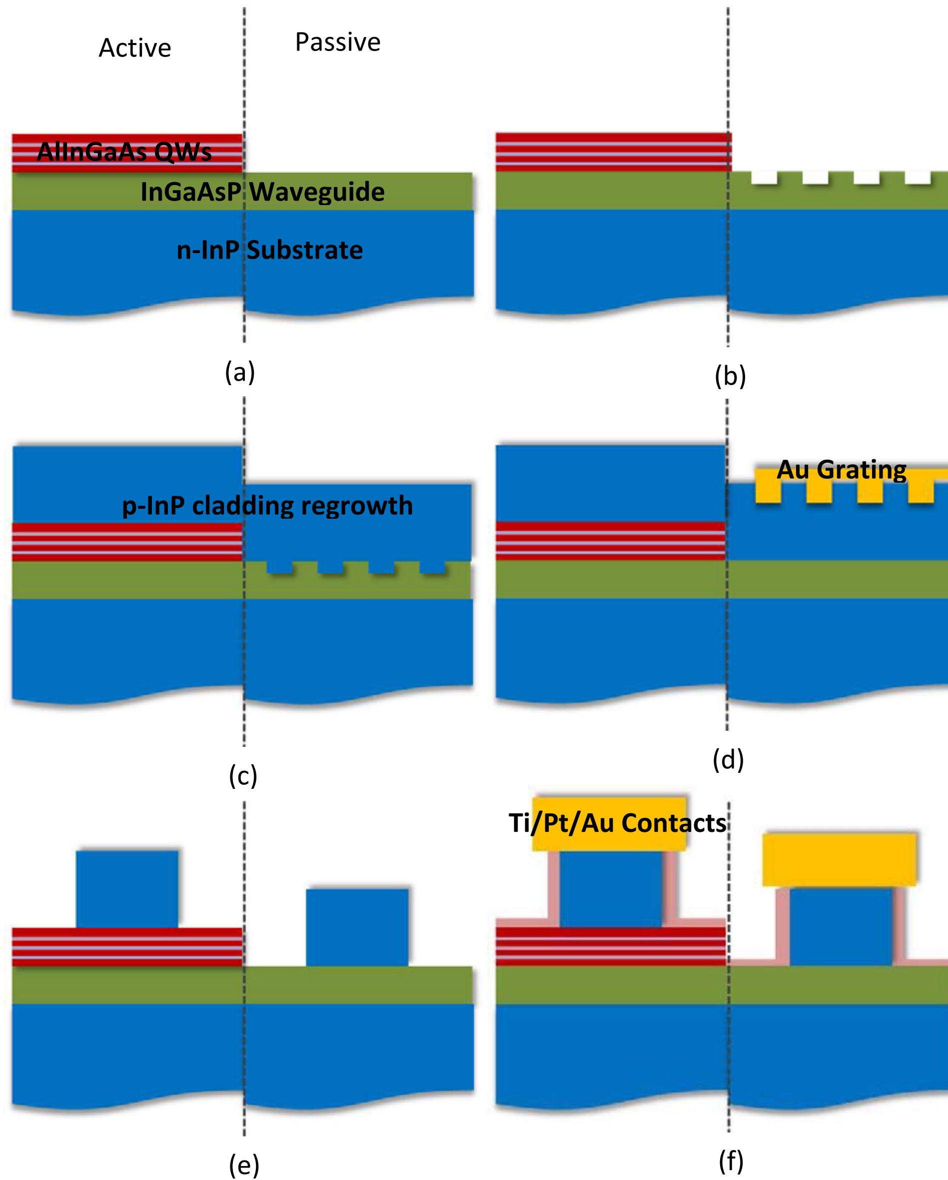


Figure 5.1 Schematics of chip topography associated with major processing steps (a) active/passive definition to remove QWs from passive areas, (b) grating etch for semiconductor mirrors, (c) InP cladding regrowth, (d) grating etch for metal grating mirrors, (e) active/passive waveguide definition, and (f) direct vias and metal contacts

5.2 Fabrication

5.2.1 Active Passive Integration

In prior work at UCSB on InP-based offset QW platforms, the QWs are compressively strained InGaAsP wells. The active/passive definition happens by masking the active areas with Si_3N_4 and wet etching the wells down to a thin InP stop layer on top of the waveguide. The wet etch chemistry is highly selective between InP and the 1.4Q InGaAsP waveguide layers, so this process works well. The QWs etch evenly with little undercut making it possible for a smooth, even regrowth[4].

This process was the starting point for the initial process development of our AlInGaAs QW platform. We began by masking the wells with Si_3N_4 and wet etching each successively layer until we reached the InP stop etch layer. The following wet etch chemistries were used: for InP, H_3PO_4:HCl 3:1, for InGaAsP, H_2SO_4:H_2O_2:H_20 1:1:10, for AlInGaAs, H_3PO_4:H_20_2:H_20 1:5:15. After this wet etch, the active mesas were severely undercut. However, there was a large amount of processing tolerance and the undercut did not appear to affect the active/passive interface near the waveguide transitions. These wet etched samples were sent for InP cladding regrowth. When the samples returned, it was clear that the regrowth was not smooth and even as we would have expected from seeing previously regrown offset QW samples. Figure 5.2 shows an SEM image of the active mesas after they returned from regrowth. From this image we could see that the active passive interface was very rough and there were small gaps in the regrowth.

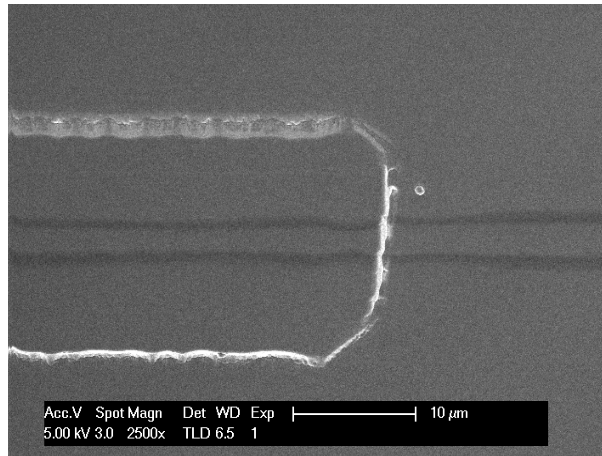


Figure 5.2 Regrown InP over active mesa defined by wet etched. Shadow is from previously removed resist.

We continued with the next processing step, waveguide definition, to see the effect of the rough active/passive transition. Again we proceeded with a the standard waveguide process of dry etching the waveguide approximately halfway and following with a H3PO4:HCl wet etch[5]. Figure 5.3 shows the results of that dry/wet etch process.

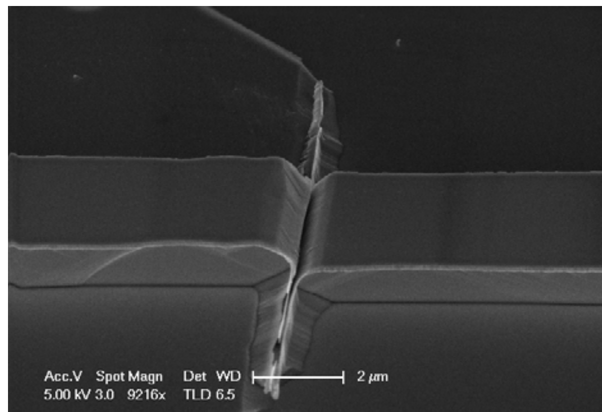


Figure 5.3 Active/passive waveguide transition at interface of regrown, wet-etched active mesa.

We can see from this image that there is a major gap in the waveguide at the active passive transition. We conjecture that the severe undercut of the wet etched active mesa caused the crystal regrowth to occur on intersecting crystal planes. Given that wet etching is highly selective to crystal geometry, the issues at the mesa interface are significantly is exacerbated by wet etching up to 50% waveguide depth. Clearly, we needed to alter the standard active mesa waveguide definition processes to suit our platform.

In order to correct the problems occurring with the active/passive definition step and subsequent waveguide definition steps, we decided to eliminate as much of the wet etching as possible. We again defined active mesas with SiN, but instead of wet etching, we used a $CH_4/H_2/Ar$ etch chemistry in RIE#2. We attempted to use laser monitoring during the dry etch to stop on the InP stop etch layer above the waveguide. The InP and InGaAsP material have an even etch rate and maintain a smooth surface during the etch, which yields nice laser monitoring conditions. However, the etch rate for AlInGaAs is much slower and the surface gets significantly roughened during the $CH_4/H_2/Ar$ etch causing the laser monitor to become unreliable. We used etch rate calculations to dry etch through the majority of the QWs. However, we stopped the etch short of the InP stop etch layer, because etching past the wells and into the 1.1 Q waveguide would be catastrophic for the devices. We followed the dry etch with a very short (< 30sec) clean up wet etch. This process yielded significantly better looking active mesas, we felt confident to move along in the process.

5.2.2 Semiconductor Gratings

Prior to the beginning of this work in metal gratings in 2007, grating patterns were formed at UCSB using holography[6]. The technique was widely used because of its low cost and ability to be used over large areas in a relatively short amount of time[7]. The major disadvantage of using holography is that is unreliable and there are often grating inconsistencies across the sample. Although electron beam lithography is a slower, more expensive process, it provides more accuracy in defining the grating pitch, high uniformity across the sample, and is very reliable. Because of its major advantages, electron beam lithography has now become the virtual standard for defining gratings at UCSB. Grating definition using EBL is extensively covered in Chapter 4, so here we will only discuss the process as it differs from the inverse patterning method used to define metal gratings.

To fabricate semiconductor grating mirrors that will be regrown, we begin by depositing a 50nm thick SiO2 hardmask on the sample. Ebeam resist (ZEP520A:Anisol 2:1) is spun on the sample and the grating pattern is defined using a pattern and exposure designed to prevent overexposure due to proximity effects. The hard mask is dry etched using CHF3 in RIE#3. The resist is stripped and the SiO2 hardmask is used to transfer the grating pattern to the semiconductor via a $CH_4/H_2/Ar$ dry etch in RIE#2. A 30 second H3SO4 etch smoothes the gratings and the SiO2 hardmask is removed in buffered HF. Figure 5.4 shows the dry etched active mesa with the etched semiconductor grating.

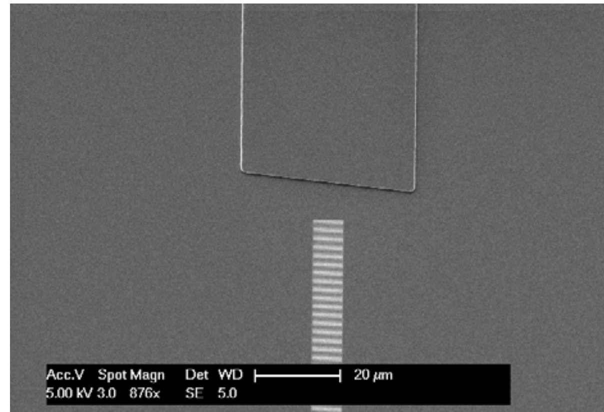


Figure 5.4 Active mesa with etched semiconductor grating ready for regrowth.

At this point, the sample is ready to be regrown with a p-type InP cladding and InGaAs contact layer.

5.2.3 Regrowth

In Section 5.2.1, we discuss early challenges associated with the regrowth process. After redeveloping the active/passive etch process, we saw significantly better regrowth quality in the second round. Figure 5.5 shows a regrown active mesa. We can see that the active/passive interface is much smoother and there are significantly fewer defects around the mesa. We anticipate that the improved regrowth will also positively affect future waveguide processing.

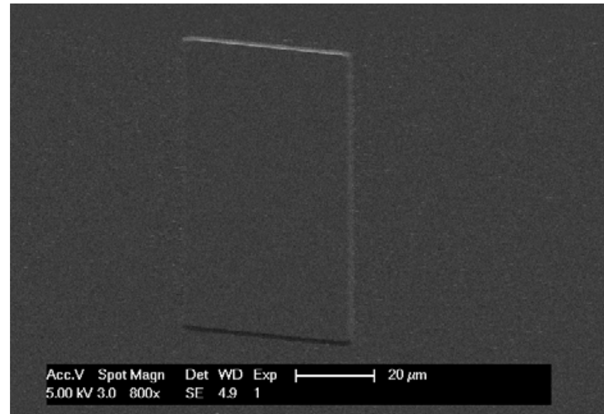


Figure 5.5 Regrown active mesa showing good regrowth quality.

5.2.4 Metal Gratings

We discuss our fabrication strategy for metal gratings extensively in Chapter 4, but we have yet to address the way those grating get integrated with optical waveguides. We experimented with two methods. The first method started with etching the waveguides using the method discussed in Section 5.2.1. Once the surface ridge waveguides and deep ridge waveguides, if desired, are fabricated, the sample undergoes the inverse patterning method to fabricate metal gratings on top of the waveguides. We found that this method yielded inconsistent grating etch results. Figure 5.6 shows a surface ridge waveguide with the grating hardmask etch. We can clearly see that large parts of the hardmask are missing and there are many defects in the gratings. This would certainly yield an even worse grating if we used this hardmask for the InP grating etch. After several attempts at this integration strategy, we modified the process.

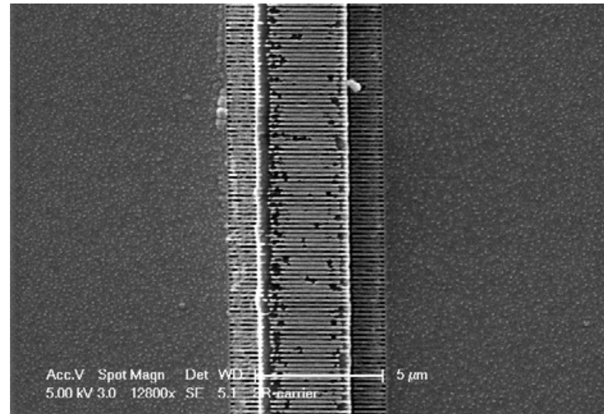
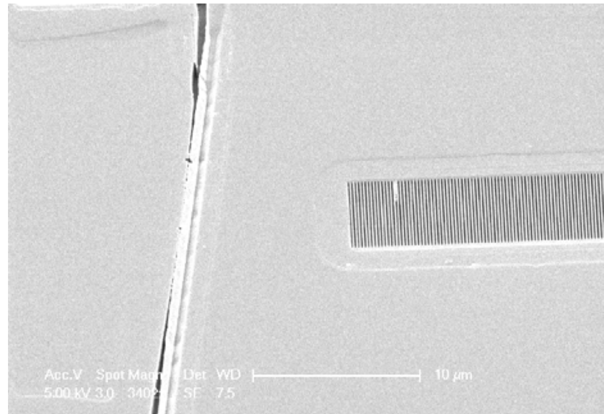
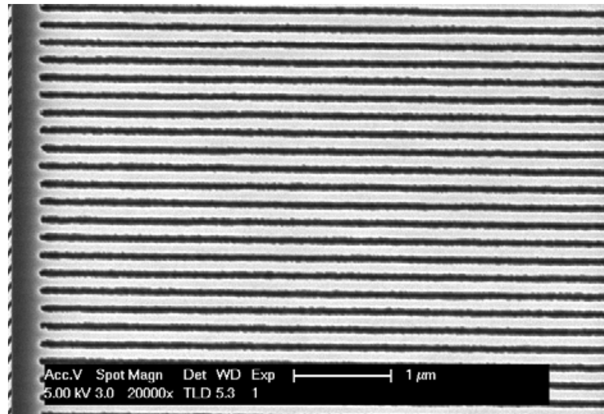


Figure 5.6 Hardmask for grating etch process showing many delamination and many defects.

The second method we used to integrate the deeply etched gratings onto the surface ridge waveguides was much more successful. After the sample returns from regrowth, we forgo the waveguide definition step and prepare the sample for the inverse grating patterning. The sample is much more planar before the waveguides have been patterned, so ebeam resist can be spun much more evenly across the surface of the sample resulting in a much higher quality grating. Figure 5.7(a) shows the deeply etched grating next to the active/passive interface. We can see that there are still defects in the etched grating, but there is a significant improvement over the previous method. The waviness seen in this grating can be attributed to very minor sub-field stitch errors in the ebeam lithography on the order of 1-2nm. Figure 5.7 (b) shows a close-up SEM image of the etched gratings. The duty cycle is less than the designed 50%, but it has been shown that this will not have a significant impact on the reflectivity of first order gratings[8].



(a)



(b)

Figure 5.7 (a) Deeply etched grating show next to active/passive mesa before waveguide definition. (b) Zoomed view of deeply etched grating.

One of the only drawbacks to patterning the grating before the waveguides is that excellent alignment between the grating and the waveguides becomes much more difficult. Both layers have to used the regrown active/passive alignment mark leaving much more room for error than aligning the grating to a freshly etch alignment mark on the waveguide layer. Overall, this alignment didn't prove to be a major problem, but this grating/waveguide integration method did make the lithography process slightly less robust.

Instead of proceeding to the sputtered metal deposition outlined as the next step in the inverse grating process outline in Chapter 4, we will first pattern the waveguides. Depositing metal in the grating at this point could lead to masking effects on the waveguide layer or increased losses by scattering metal over the sample.

5.2.5 Waveguides

After the issues encountered with the waveguide etching during the first regrowth process discussed in Section 5.2.1, we decided to modify the waveguide etch to require less wet etching. While the improved active/active passive process would have likely solved most of the waveguide etch issues, we decided to take extra precaution to ensure better waveguide transitions between the active and passive material. Instead of dry etching the waveguide by approximately 50% and wet etching the rest of the way to the waveguide layer, we used laser monitoring to increase the dry etch depth to 75% of the waveguide height and follow up with a shorter wet etch. The waveguides were dry etched in RIE#2 with a $CH_4/H_2/Ar$ etch chemistry and followed up with the standard InP H_3PO_4:HCl wet etch .

Figure 5.8 shows an SEM image of the surface ridge waveguide fabricated over the active passive transition. We can see that the ridge transition is much smoother and very comparable to other fabrication results achieved at UCSB[1]. We still see some sidewall roughness, which is likely the result of the longer dry etch.

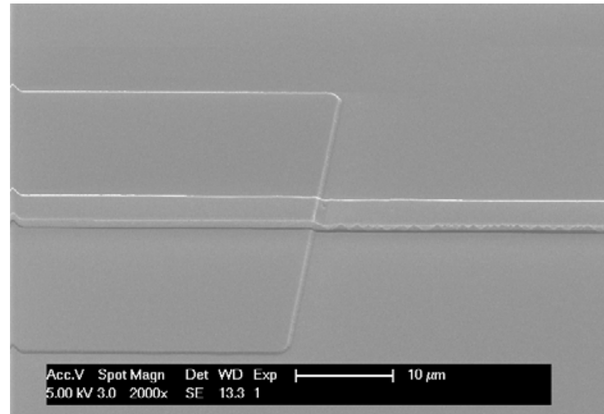


Figure 5.8 Surface ridge waveguide with improved active passive transition.

Cross-sections of the active and passive surface ridge waveguides can be seen in Figure 5.9. The active waveguide shown in Figure 5.9(a) is shown after the contact metallization step. Both the active and passive waveguides show undercut from the wet cleanup etch. This affects the confinement factor of the active mode in the quantum wells, as well as increases scattering loss in both waveguide structures. We expect this to negatively affect the performance of devices by increasing the internal cavity loss of the lasers.

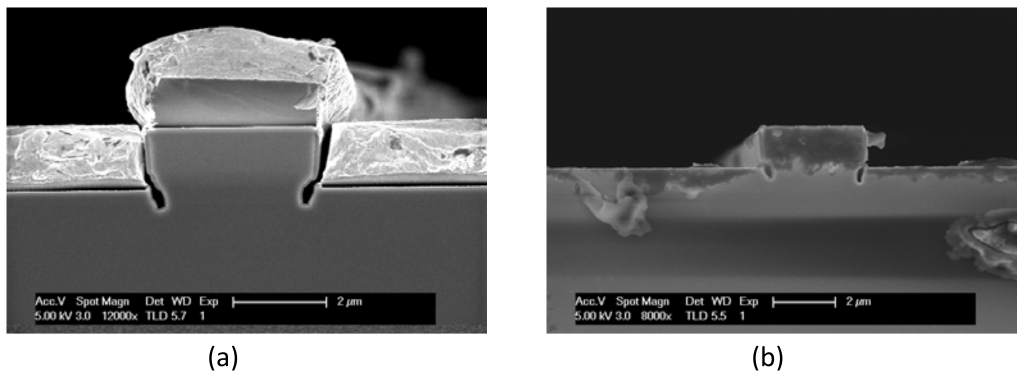


Figure 5.9 (a) Cleaved cross-section of active surface ridge waveguide with contact metal. (b) Cleaved cross-section of passive surface ridge waveguide. Undercut can be seen in both waveguides.

As discussed in Section 5.2.4, the deeply etched gratings were fabricated on the sample before the waveguide layer was defined. Figure 5.10 shows the grating patterned on top of the etched waveguide. We can see that the grating etch depth is about 300nm. This is short of the targeted 500nm etch depth. There are also unetched strands of semiconductor material that were not cleaned up during the wet etch. Overall, the integrity of the grating was maintained very well.

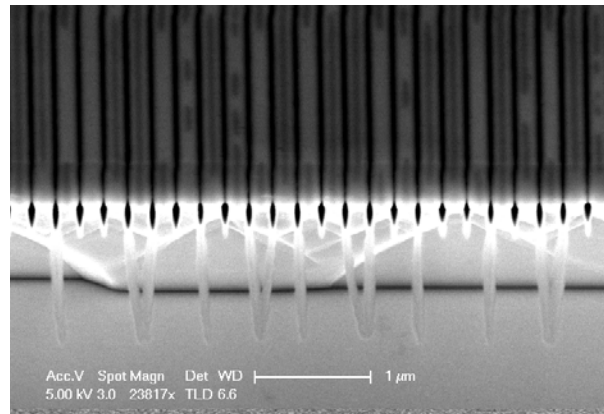


Figure 5.10 Waveguide shown with deeply etched InP grating.

After the waveguides are defined and the sample as been cleaned and stripped of any hardmasks, metal can be sputtered into the deeply etched InP gratings. This is done by spinning the sample with a bi-layer resist designed for liftoff. The resist is opened over the gratings with traditional optical lithography. Gold is sputtered over the entire sample at a rate of 2 angstroms/second. This slow deposition rate is necessary to ensure that the gold fills all of the openings in the grating. After the metal deposition, the sample is soaked in acetone to remove the gold from the

majority of the sample. In general, sputtering is not an ideal technique for liftoff. It works in this instance because the bi-layer resist is thick compared to the 500nm of gold we are depositing. This technique would not be recommended for greater metal thicknesses. Figure 5.11 shows the waveguide with metal sputtered into the grating. We can see that there is some misalignment between the metal and the grating. The gold also overlaps the sides of the waveguide. We would expect that this would increase the internal losses of the laser.

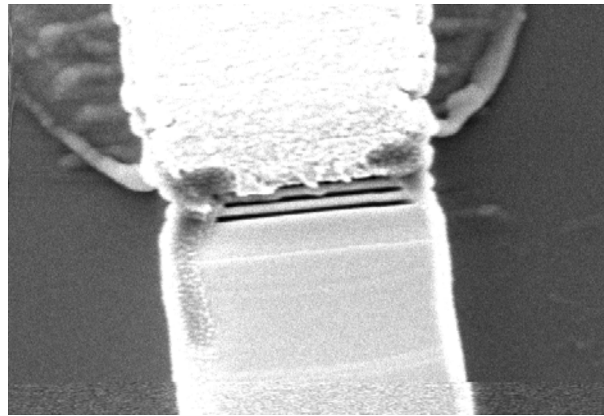


Figure 5.11 Waveguide shown with deeply etched InP grating and metal deposition.

While it was not a necessary feature for the devices reported in this dissertation, we also demonstrated that a passive deeply etched waveguide can be integrated into this platform. Specific processing steps can be found in Appendix A, but here we show the fabricated waveguide structures. Figure 5.12(a) shows the surface ride to deep ridge transition of the passive waveguide while (b) show the cleaved cross-section of the deeply etched waveguide.

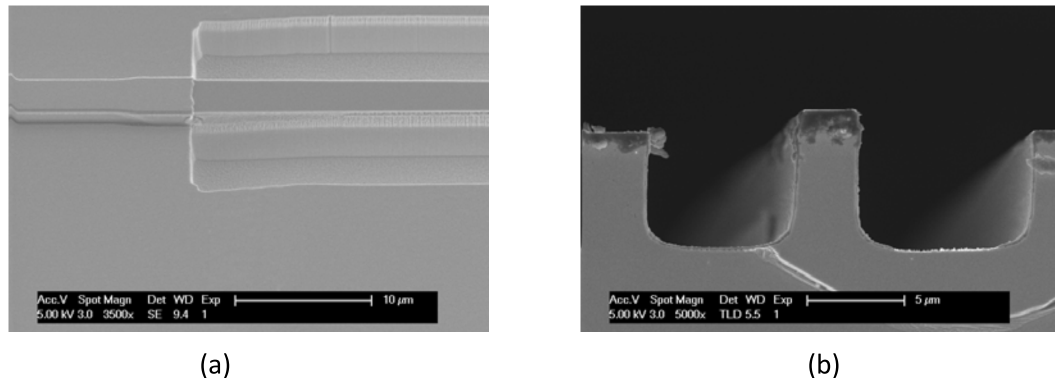


Figure 5.12 (a) Passive waveguide surface ridge to deep ridge transition. (b) Cleaved cross-section of deep ridge waveguide

5.2.6 Contacts

After the waveguide fabrication and grating metal deposition, metal contacts for current injection are the final top-side fabrication step. The sample is coated with SiN and direct vias are opened over the active waveguides. The contact metal layer stack deposited is Ti/Pt/Au with thicknesses of 200Å/400Å/13000Å, respectively. Liftoff removes the excess metal from the sample. Figure 5.13 shows an SEM image of the part of one die on the sample after the contact metal processing step. Figure 5.14 shows closer views of the devices after top-side processing has been finished. After the top-side p-contacts were fabricated, the sample went through the standard thinning and back-side n-metal contacts[1].

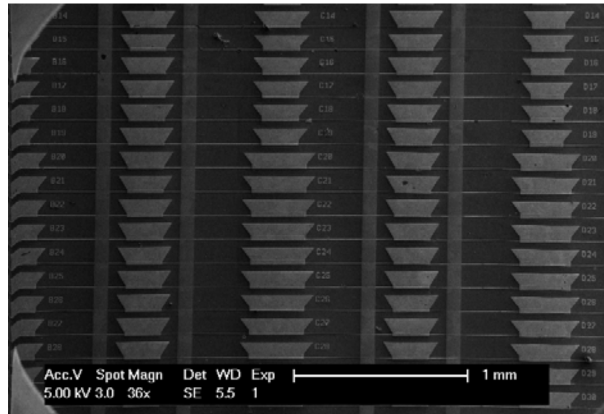


Figure 5.13 View of many devices after top-side contact metal processing.

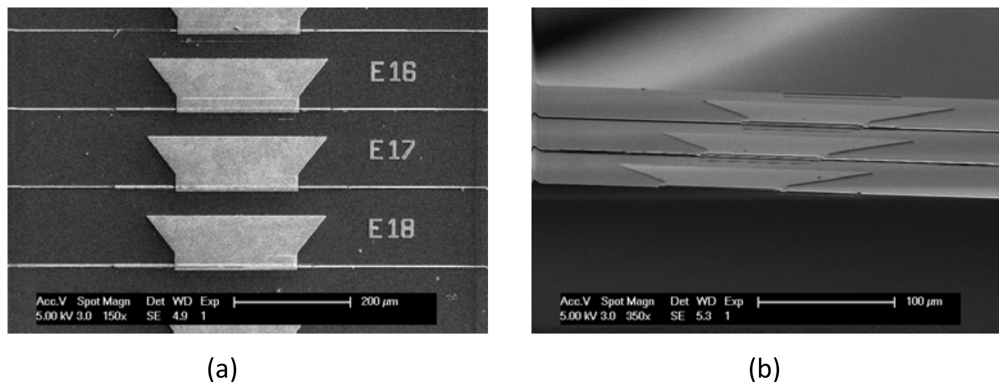


Figure 5.14 (a) DBR laser with two metal mirrors after top-side processing is complete. (b) Angled view of lasers showing device topography.

Contact metal deposition is one of most standard parts of this fabrication process, but it can drastically affect the yield of working devices. In this case, there was an issue with metal coverage extending between the top of the ridge where current is injected and the probe pad. This resulted in some dies having up to 60 percent open circuit devices. This issue with the contacts greatly contributed to very low yield for these devices. We recommend using a low deposition rate of

approximately 8-10 angstroms/sec for gold to increase the number of working contacts.

5.3 Integration and Yield Issues

This fabrication effort has made major developments in creating devices designed for the highly tensile strained AlInGaAs material platform. However, despite the enormous amount of time and effort put into developing a working fabrication process, there were some significant issues that we encountered that adversely affected device integration and yield. One of the most debilitating and frequently recurring issue was finding suitable etch chemistries for both wet and dry etches. Many of the wet etches were not selective enough with regards to the material. This can be seen in Figure 5.2 and Figure 5.10 with the active mesa and waveguide undercut, respectively. We also found that the $CH_4/H_2/Ar$ dry etch chemistry was too selective between InP and AlInGaAs. Figure 5.15 shows that during the deep etch process, the passive waveguide sections etched nearly 3 times as quickly as the active region. This proved prohibitive in two ways. First, during the active passive dry etch, a large amount of polymer accumulated on the sample due to the necessity of a lengthy etch time. This etch rate differential was also prevented us from properly fabricating some experimental laser designs unreported in this dissertation. A chlorine based dry etch chemistry would likely go a long way in solving the issue of the etch rate differential. While that functionality is available at UCSB, it was unfortunately inaccessible during the time these devices were fabricated due to equipment failure.

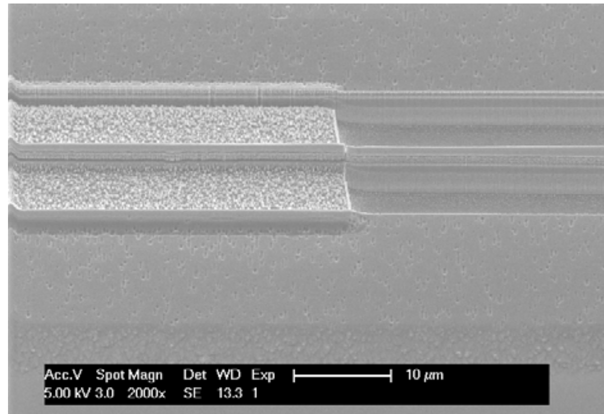


Figure 5.15 Waveguide deep etch demonstrating the material selectivity of the $CH_4/H_2/Ar$ dry etch chemistry.

Another major issue with this fabrication process was device yield. While yield is not typically a considered a major problem when fabricating novel devices to demonstrate proof of concept, it did prove prohibitive in this case because we couldn't do a full characterization of the devices because the device yield was so low. The vast majority of the yield issues stem from the poor metal coverage during the contact metal deposition discussed in Section 5.2.6. However, there were many instances of nano-scale grating features being broken or destroyed during the micro-scale fabrication of waveguides. More discussion of how to address these issues takes place in Chapter 7, but improvements do need to be made to allow for device sophistication and performance to advance.

5.4 Summary

In this chapter, we have demonstrated the fabrication of DBR lasers with metal and semiconductor grating mirrors. We began the processing with a standard UCSB

fabrication plan for InP-based materials. However, in order to fabricate our devices to specification, we needed to re-develop significant parts of the process. The active/passive interface etch was transformed from a complete wet etch to a dry etch with a very short wet, clean up etch. This greatly improved the quality of the regrowth. The waveguide etch and metal grating/waveguide integration were also redeveloped to be more supportive of the material platform and the integration of micro-scale and nano-scale features. Although, it was not used for the named devices, we also showed that a deeply etched waveguide architecture could be fabricated on this platform. Very little previous work had been done to use this tensile strained AlInGaAs QW structure to make grating lasers. While there are dry etches in this process that could benefit from updated etch chemistries, major steps have been made to demonstrate the capabilities of this platform.

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Chapter 6

Device Characterization and Results

In this chapter, the performance of a distributed Bragg reflector (DBR) laser with metal grating mirrors is presented. The power-current-voltage (LIV) data is reported and the optical spectrum is shown for lasing operation. We discuss and compare the effect of individual components of the laser designs on experimental lasing parameters. Finally, we discuss the feasibility of using sub-wavelength metal gratings as in-plane laser elements.

6.1 Testing Setup

After device fabrication, the individual laser bars were cleaved apart and soldered on aluminum nitride (AlN) carriers. The AlN carriers are coated with gold with the top side of the carriers acting as the ground plane for the soldered devices. The carriers are mounted to the copper testing stage with thermal paste to ensure even cooling over the sample. Light generated by the laser was collected off-chip with lensed optical fiber on both cleaved facets of the lasers. The cleaved facets were not AR coated, maximizing the intensity of the stimulated emission measured out of the laser[1].

The laser results shown in this chapter were all measured under pulsed operation at 18°C unless otherwise noted. The pulses were 1 μs in duration with 1 μs of off time, a 50% duty cycle. The devices were tested for CW operation, but they failed to lase. We attribute this to internal heating and internal loss. This was predicted after the Fabry-Perot lasers demonstrated a gain peak shifted to 1330nm, far away from the design wavelengths of 1290nm-1310nm.

6.2 Distributed Bragg Reflector Lasers with Metal Mirrors

As part of the first step proof of concept, the most basic active device we chose to fabricate is a DBR laser with an active cavity and two passive metal mirrors. We designed iterations of the laser with a wide variation of device parameters. Cavity lengths, grating pitch, and mirror length were all varied to demonstrate and characterize the potential performance capacity for these devices. Due to several issues including fabrication yield, discussed in the previous chapter, we only had a few working devices. Those working devices did lead us to two important outcomes: (1) a proof of concept was established that metal grating can act as laser mirrors and (2) we were able to attribute laser performance to specific elements of the devices.

The best working DBR laser with two metal mirrors is presented here. The laser presented has a 300 μm long active cavity. The front mirror is 100 μm long and the back mirror is 200 μm long. Both gratings are designed with a 202nm pitch, which should yield a lasing wavelength of 1310nm. Figure 6.1 shows the LIV performance curves of the laser taken at 18°C. As can be seen from the figure, the

laser threshold is conservatively gauged to be 75mA with a maximum output power of 11.7 μW.

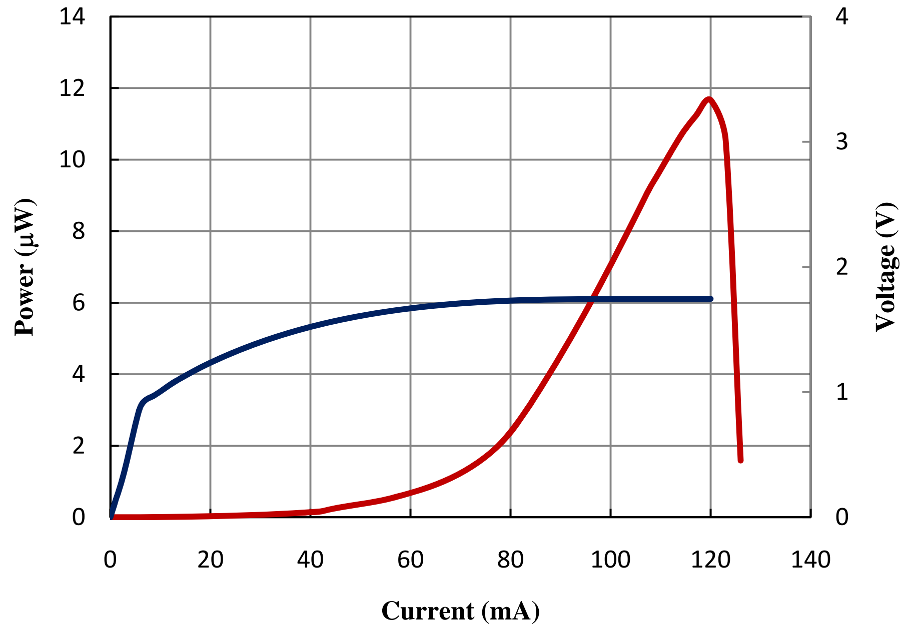

Figure 6.1 LIV curves of pulsed lasing operation of DBR laser with two metal mirrors.

Using equation 6.1, we can calculate the differential quantum efficiency of the laser to be 0.06 %.

$$\eta_d = [\frac{q}{h\upsilon}]\frac{\Delta P_o}{\Delta I} \qquad (6.1)$$

At higher injection currents, the slope efficiency rapidly drops. It is likely that this happens as a result of heating in the device, although thermal roll off is typically a more gradual effect[2].

Because of the very small number of working devices, it is very difficult to get a good estimate of $<\alpha_i>$ for the DBR lasers. The $<\alpha_i>$ from the broad area lasers measured in Chapter 4 is 16.41 cm^{-1}. The injection efficiency was calculated to be 61%, which is fairly low and may explain the low $<\alpha_i>$ value for the broad area lasers. Regardless, the value for $<\alpha_i>$ indicates that the material loss is within a reasonable range. The modal gain confinement factor is also affected by the undercut waveguide. For an ideal active, surface ridge waveguide we calculate the confinement factor to be 7%, but recalculating to account for the undercut gives a lower confinement factor of 5%. Given the extremely low value measured for differential quantum efficiency of the DBR laser, we can assume that $<\alpha_i>$ or $<\alpha_m>$ are higher in the DBR lasers compared to the broad area lasers. This increase can likely be attributed in part to additional scattering and loss caused by the undercut waveguide and the optical loss from the metal. More likely, the mirror loss of the gratings is higher than predicted, and we will discuss this in more detail later in the section.

Figure 6.2 shows an IR image of the reported device under pulsed operation. We can clearly see the optical intensity is centered in the laser cavity with a fair amount heat spreading.

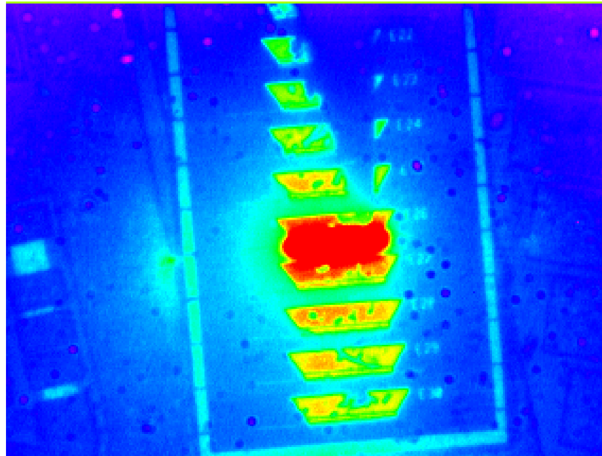

Figure 6.2 IC camera image taken during pulsed lasing operation of DBR laser with two metal mirrors.

Light was measure out of both sides of the laser, but negligible amounts of light were collected from the front mirror. This can also be seen in Figure 6.2. This leads us to conclude that there is some inconsistency in the device cleaving or grating fabrication.

Figure 6.3 shows the optical spectrum of the laser measured with an optical spectrum analyzer with a sensitivity of 0.7nm. A single mode at 1311.7nm shows 11dB of suppression over the baseline ASE. This laser was designed with a 200 micron long left mirror and a 100 micron long right mirror. The grating period was designed for lasing at 1310 nm. We can see from the spectrum that the measure peak wavelength is very close to specification and could be tuned closer to 1310nm with additional cooling.

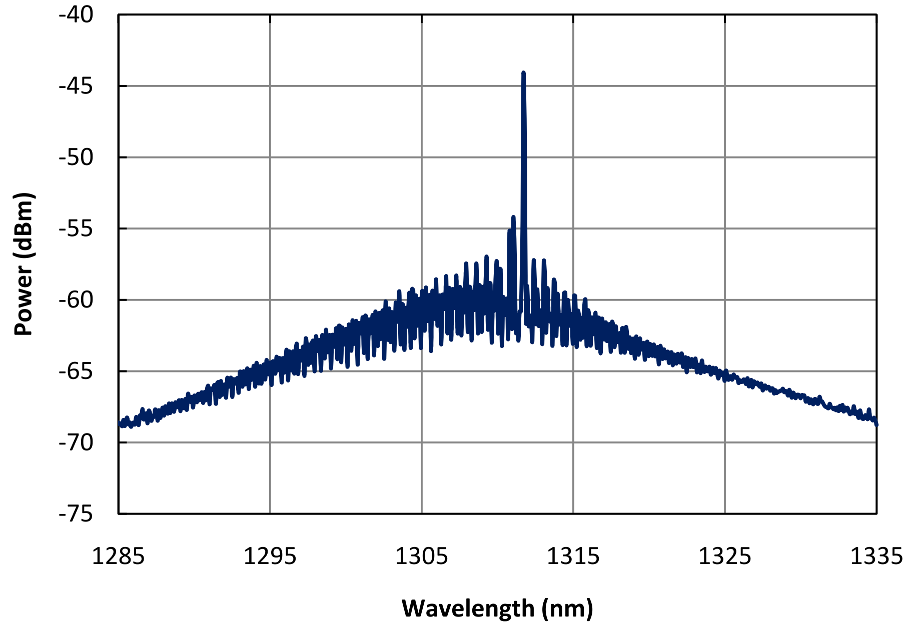

Figure 6.3 Optical spectrum of DBR laser with two metal mirrors lasing operation at 80mA.

Since these lasers were cleaved away from their on-chip detectors and the facets were not AR coated, we will do some additional analysis to determine that the lasing is at least partly attributed to the grating mirrors, and not the cavity defined by the cleaved facets. There is already some evidence to show that the gratings are performing as in-plane DBR mirrors. First, we can see that the shape of this optical mode spectrum looks different than the Fabry-Perot spectrum seen in Chapter 4. Additionally, lasing was not achieved under CW for this laser. There is clearly frequency selection occurring in the spectrum and given that the peak lasing mode is so near the design wavelength, the gratings are clearly acting as more than metal slab reflectors, and are collectively reflecting a few select wavelengths.

However, there are certainly coupled cavities in this laser due to the cleaved facets and multiple grating mirrors. Figure 6.4 shows a zoomed in image of a cleaved cavity very similar to the one reported in this section. There are 6 total cavities for this device, but since the laser cavity is centered between the facets, we should see resonances in the lasing spectrum from four different cavity lengths. The four cavities, labeled A-D are defined by the following mirrors: cavity A – cleaved facet to left metal mirror, cavity B – left metal mirror to right metal mirror, cavity C – cleaved facet to right metal mirror, and cavity C – cleaved facet to cleaved facet.

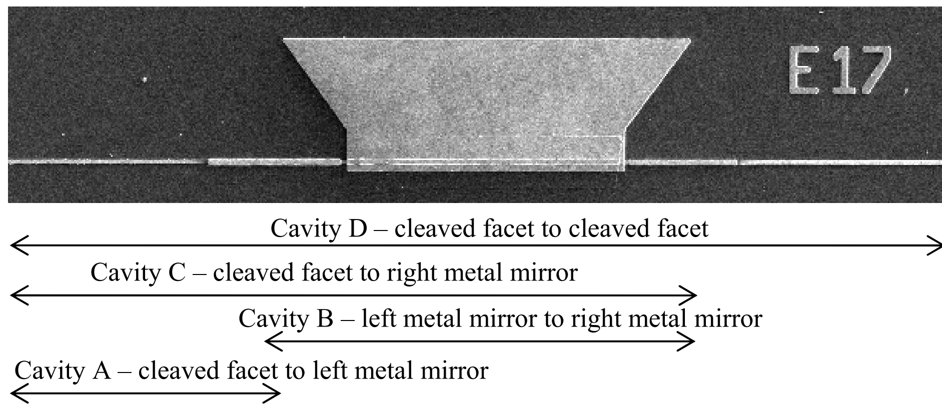

Figure 6.4 Image of cleave cavity with DBR laser. Four coupled cavities are defined.

In order to analyze the cavity resonances in the lasing spectrum to determine that gratings were acting as laser mirrors, we performed a fast Fourier transform (FFT) on the spectral data[3]. The results are seen in Figure 6.5. The resonances are labeled A-D to correspond the cavities defined in Figure 6.4.

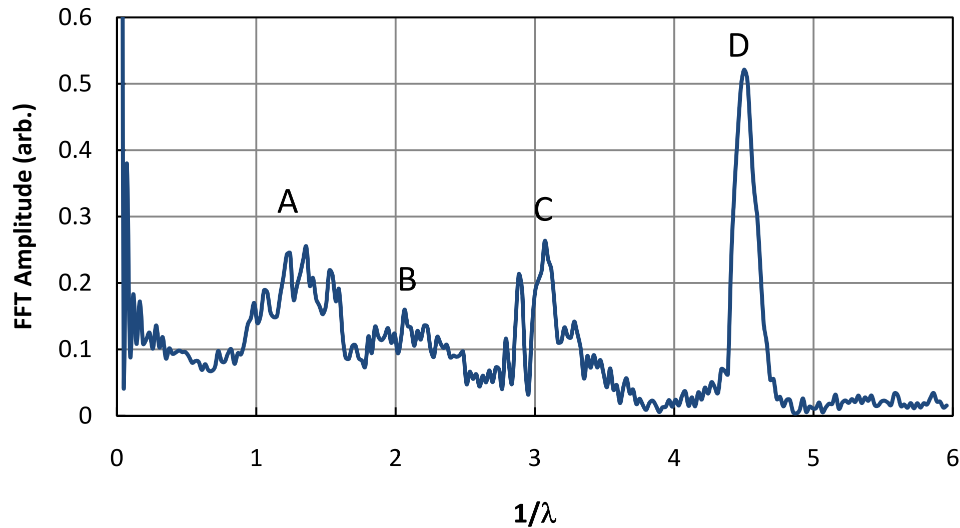

Figure 6.5 Fast Fourier transform of optical spectrum data to determine cavity resonances.

We can see from the FFT data that resonances from the four cavities we expected to see are present. We can use the active group index we measured from the Fabry-Perot lasing data and an estimated passive group index to determine the cavity lengths[4]. One added benefit to this approach is that we can also accurately determine the effective mirror length of the gratings and extract out the actual reflectivity of the gratings.

For cavity A, the peak 1/λ spacing is 1.21 which corresponds to a cavity length of 259 microns. This cavity is defined by a cleave facet and a grating, where the distance between the cleaved facet and the leftmost edge of the grating is 165 microns, giving us an effective mirror length of 96 microns for a 200 micron long grating. We can calculate the grating coupling coefficient, kappa, using Equation 6.2.

$$L_{eff} = \frac{1}{2\kappa}\tanh(\kappa Lg) \tag{6.2}$$

The kappa for the left grating is ~ 25 cm-1, which is much lower than we expected. This means that the reflectivity of a single grating period is 0.00025 and the reflectivity of the grating is ~ 0.462. This corresponds to a calculated grating etch depth of ~200 nm. If we perform the same calculations on cavity C, another cavity with one grating mirror and one cleaved facet, we determine that the effective mirror length for the 100 micron long mirror is 49 microns. This agrees with the previously calculated values of kappa and single grating period reflectivity. The corresponding reflectivity of the right metal mirror grating is calculated to be ~ 0.24.

In order to double check these calculated results, we will compare the effective mirror length values to those of cavity B, the DBR laser cavity defined by two metal mirrors. The $1/\lambda$ spacing of the FFT chart is 2.09 and this corresponds to a cavity length of 447 microns. This result shows close agreement with the previous calculations indeed confirming our low kappa value of ~ 25 cm^{-1}. The final FFT resonance corresponding to cavity D has a $1/\lambda$ spacing of 4.57, which corresponds to a cavity length of 1034 microns. This is indeed the length of the cavity defined by the cleaved facets.

It is worth noting that the resonance for cavity D is likely more clearly defined and has a higher amplitude than the other resonances due to the fact that the cleaved facets have a broader reflectivity spectrum. The cleaved facets are also a single reflection, as opposed to a collective reflection from many grating periods so the resonance is caused by a more well defined distance.

6.3 Hybrid Distributed Bragg Reflector Lasers with One Metal Mirror

Beyond our initial proof of concept that an integrated laser could be made with two metal grating mirrors, we wanted to compare the performance of metal grating mirrors to semiconductor regrown mirrors commonly associate with InP grating based lasers. We designed a hybrid DBR laser with one metal mirror and one semiconductor mirror. Similar to the DBR lasers with two metal mirrors, design iterations of the hybrid DBR included a wide variation of device parameters. Cavity lengths, grating pitch, and mirror length were all varied to demonstrate and characterize the potential performance capacity for these devices. Again, there were the same issues with yield and performance experienced with other device, so we only had a few working devices. Working lasers did demonstrate that metal mirrors and semiconductor mirrors could be integrated into a single device.

The best working hybrid DBR laser with one metal mirror and one semiconductor mirror is presented here. The laser presented has a 300um long active cavity. The metal mirror is 50um long and the semiconductor mirror is 200um long. Both gratings are designed to yield a lasing wavelength of 1300nm. This translates to a 201nm pitch for the metal grating and a 200nm pitch for the semiconductor grating. Figure 6.6 shows the LIV performance curves of the laser taken at 18 °C. As can be seen from the figure, the laser threshold is conservatively gauged to be 59 mA with a maximum output power of 10.1μW. The LIV curve also shows that this laser demonstrates some instability likely due to heating.

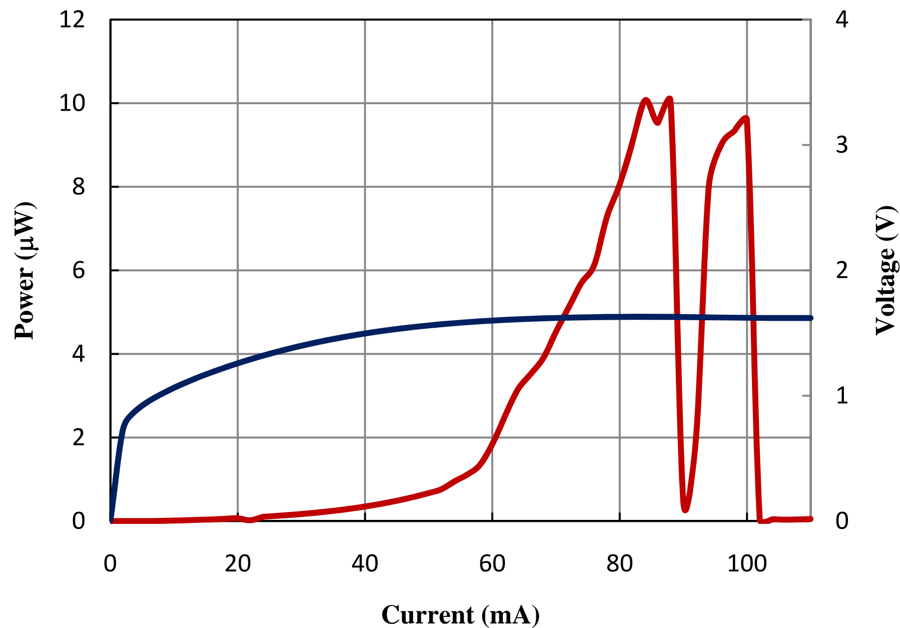

Figure 6.6 LIV curves of pulsed lasing operation of hybrid DBR laser with one metal mirror and one semiconductor regrown mirror.

Using the same method to calculate the differential quantum efficiency as for the laser shown in Section 6.2, we find the differential quantum efficiency to be 0.075%. Again, this number is quite small, but shows improvement from the first DBR laser with two metal mirrors. Given that the laser cavity is the same length as the previously reported laser and the devices came from the same die, we can assume that the injection efficiency and internal loss the increase in differential quantum efficiency is the result of lower internal mirror loss. This conclusion makes senses given that the optical mode is only contacting one metal grating as opposed to two. We would expect the total losses incurred from the mirror material losses to be lower.

Figure 6.7 is an IR image of the laser under pulsed operation. Again we can see that the optical intensity is centered in the laser cavity. Ninety-five percent of the

light collected from this device was from the facet with the semiconductor grating mirror.

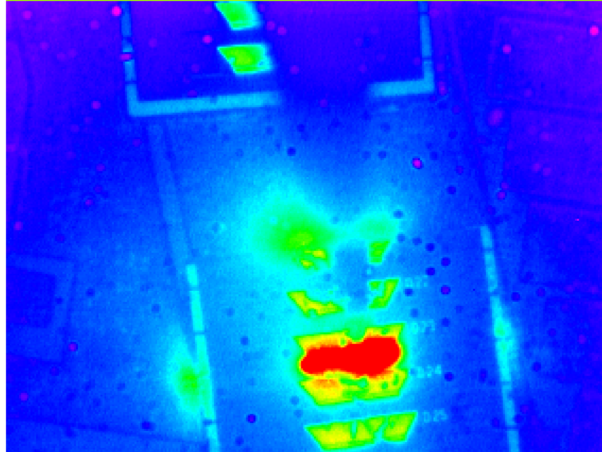

Figure 6.7 IC camera image taken during pulsed lasing operation of DBR laser with two metal mirrors.

Figure 6.8 shows the optical spectrum of the laser measured with an optical spectrum analyzer with a sensitivity of 0.7nm. This optical spectrum has two distinct features. The first is a lasing mode at 1304.1nm with 20 dB suppression of side modes. The second distinct feature looks like a band pass filter in the ASE at 1292.7nm. One major take away from this lasing spectrum is that the Bragg wavelength of the semiconductor grating and the metal grating are mismatched. This can be attributed to working with a new material platform that has a different effective index of refraction than expected. Additionally, the calculated effective index of the metal grating will be inaccurate because of the shallow etch depth.

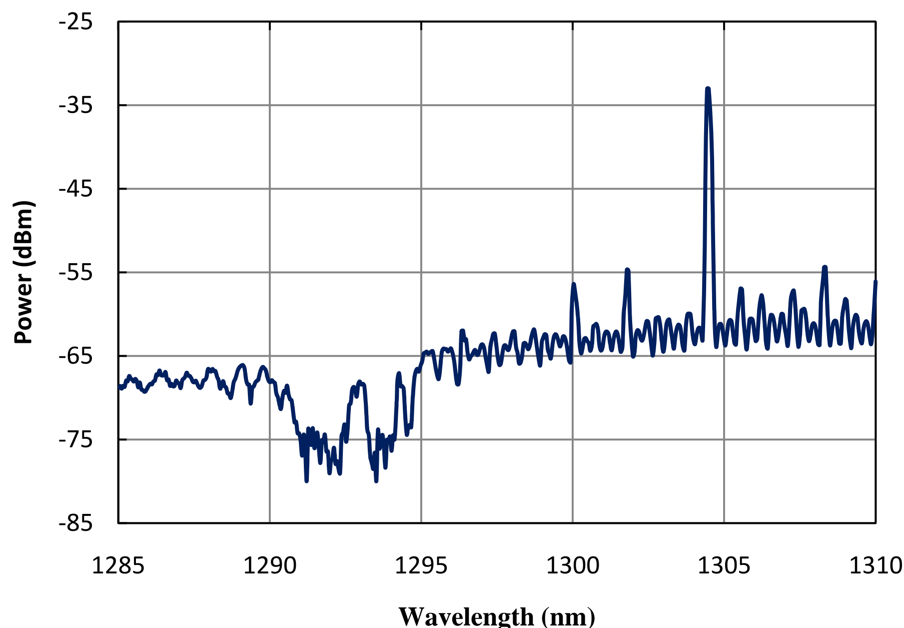

Figure 6.8 Optical spectrum of DBR laser with one metal grating mirror and one semiconductor grating mirror under lasing operation at 80mA.

Figure 6.9 shows a closer view of the lasing modes in the optical spectrum of the hybrid DBR laser over a range of temperatures. We can see that as the temperature changes, power is shifted between lasing modes. We postulate that as the laser is heating, the mismatched mirrors are tuning at different rates altering overlap of their reflectivity spectrums. While this device is did not perform as we designed, with some minor design changes, we show that metal grating mirrors and semiconductor grating mirrors can be integrated into the same laser.

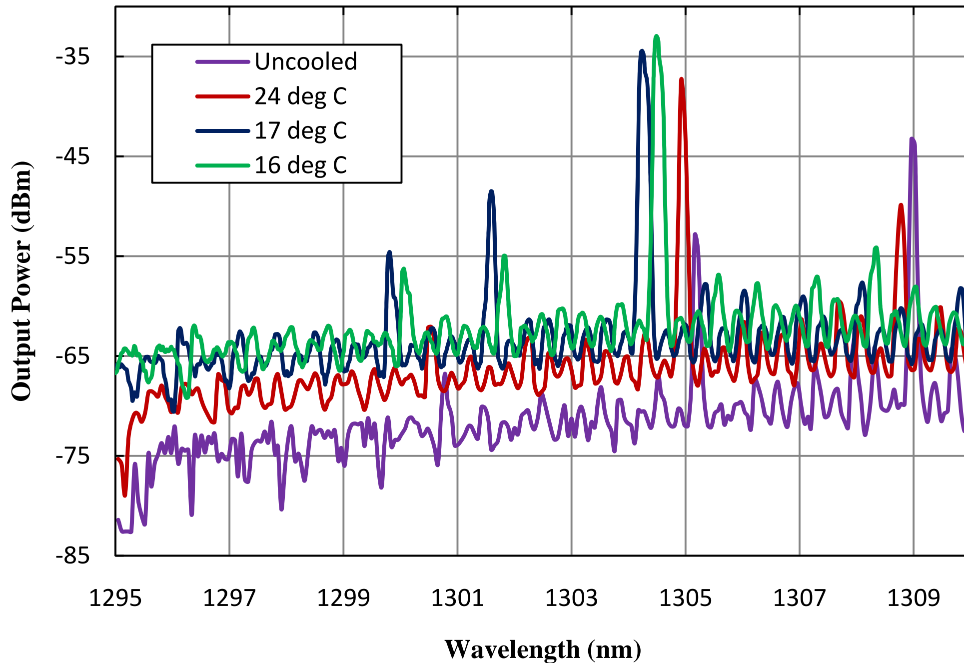

Figure 6.9 Optical spectrum of DBR laser with one metal grating mirror and one semiconductor grating mirror under lasing operation at 80mA over a range of temperatures.

6.4 Feasibility

The first priority of this work was to prove that metal gratings could be used as integrated optical circuit elements. The experimental results presented in this chapter demonstrate that in-plane lasers can be fabricated with metal grating mirrors. While this proof of concept is intrinsically interesting, we must also question the feasibility of further integrating metal gratings into optical circuits. In their current state, there is little reason to choose a metal grating mirror over a semiconductor grating mirror. While it seems that some reduction in footprint could eventually be achieved, it does not justify the huge reduction in differential efficiency of the laser. However, our

demonstration does open up new design space for integrated optical circuits, particularly in the area of plasmonic/photonic integration. If a semiconductor mirror is simply not a valid design choice, it is feasible to use a metal grating mirror provided design and fabrication can be tightly controlled.

In order to advance metal grating mirrors to the point that they would be a valid design choice for very small cavity lasers, we must be able to achieve very high reflectivity mirrors[5]. Figure 6.10 shows a plot of threshold current vs. cavity length for several mirror reflectivities for our current devices. We can see from our demonstrated laser that, at the reflectivites we are currently achieving, it would be impossible to shrink the cavity below 100 microns. The only way we are going to be able to achieve lasing in small cavities with reflectivities near or about 0.9. This should be possible with metal gratings, but it will require better fabrication reproducibility and a well understood design space. Fortunately, we have taken a step in that direction with this work.

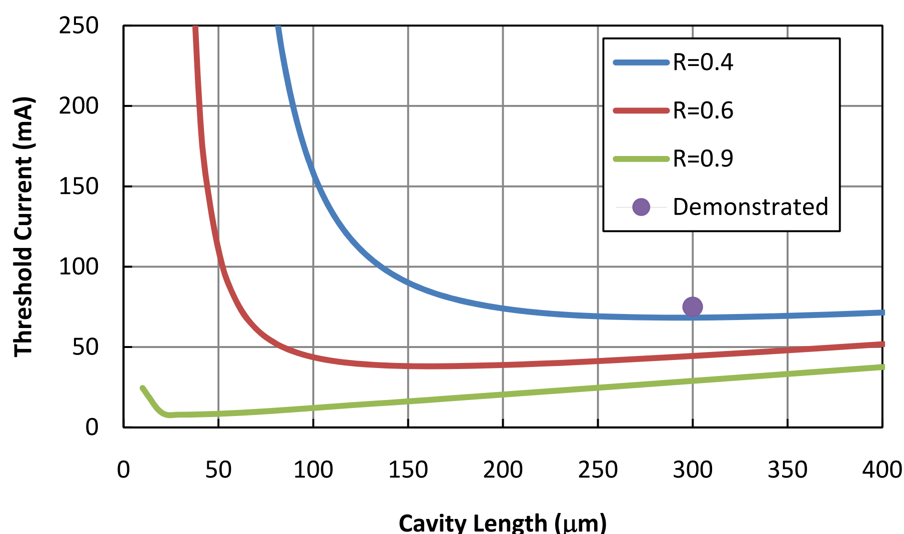

Figure 6.10 Plot comparing threshold current to cavity length for various mirror reflectivities

6.5 Summary

We have demonstrated the operation of distributed Bragg reflector (DBR) lasers with metal grating mirrors. Maximum output power ranges from 10-14 uW with differential efficiencies of 0.06-0.075%. The inefficiency of these lasers can mainly be attributed to high mirror losses, as well as losses incurred when the optical cavity mode contacts the metal gratings. Single mode lasing is demonstrated in DBR lasers with two matched metal grating mirrors. We have shown proof of concept that sub-wavelength metal gratings can serve as integrated optical circuit elements, but without major reduction in losses, they should only be used in cases where other mirror options are not valid design choices. The devices were designed with consideration given to likely applications areas where metal grating mirrors would be required. Near-term integration is demonstrated to be feasible for such applications.

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Chapter 7

Summary and Future Work

The work presented in this dissertation makes two main contributions to advance the development of photonic integrated circuits. The first contribution is the development of novel fabrication technology for integrated sub-wavelength metal gratings and in-plane grating based lasers on a tensile strained AlInGaAs quantum well platform. The second contribution is a better understanding of potential advantages and challenges of implementing metal gratings as mirrors and optical circuit elements. We discussed several different aspects of the theory, fabrication, and measurement of sub-wavelength, and while this work followed a somewhat non-linear path from conception to implementation, we now better understand why and how we should use metal gratings in photonic integrated circuits.

7.1 Dissertation Summary

In this dissertation, we explore the near-term and future potential of sub-wavelength metal gratings as optical circuit elements and in-plane laser mirrors. We begin by reviewing the theoretical and experimentally demonstrated capabilities of patterned metals. Promise has been shown in plasmonic application areas like mirrors, couplers, waveguides, and lasers, as well as left-handed materials and sensing. While the range

of applications is quite diverse, some design considerations remain fairly constant when it comes to exploiting the novel optical properties of metal gratings. Feature size must be much smaller than the desired wavelength of operation and TM mode polarization is often required to achieve unique transmission properties. We decide to focus on the potential impact of metal gratings on on-chip slow light applications keeping in mind their other potential application areas.

After determining that sub-wavelength metal gratings show promise to achieve novel on-chip manipulation of light, we proceed to discuss methods to fabricate sub-wavelength metal gratings on-chip. The challenges associated with fabricating sub-wavelength scale metal gratings that can be integrated with a wide variety of material platforms include difficulty dry etching robust metal features and achieving high aspect ratio structure on the nano-scale. As a solution, we present a fabrication approach we call the inverse patterning method. The inverse of the desired grating pattern is etched into a semiconductor or dielectric through the steps of electron beam lithography, multi-layer hardmask etching, and a deep grating etch. Then metal is sputtered into the inverse grating creating the initially desired metal pattern. The inverse pattering method was verified as an accurate fabrication technique through AFM measurement and a grating diffraction experiment. We use the presented method to fabricate metal gratings on an ultra-low-loss Si3N4 waveguide platform Experimenting with the optical transmission through the gratings leads us to determine that metal gratings possessed more near-tern potential as compact, integrable mirrors for photonic integrated circuits.

Incorporating the nearly universal design considerations we found to be true for sub-wavelength metal structures, we design distributed Bragg reflector lasers to demonstrate the potential for photonic circuit integration. An InP-based material platform is chosen along with highly tensile strained AlInGaAs QWs to provide TM gain. We use basic in-plane laser design concepts to design DBR lasers with a wide variation of parameters. Grating pitch, mirror length, cavity length, and mirror material are all varied to provide optimal opportunity for proof of concept. The resulting devices are laid out with the option to use on-chip detectors or to cleave out the lasers and measure light off chip.

We demonstrate the fabrication of DBR lasers with metal and semiconductor grating mirrors. In order to fabricate our devices to specification, we re-developed significant parts of the standard UCSB InP fabrication process. The active/passive interface etch was transformed from a complete wet etch to a dry etch with a very short wet, clean up etch. This greatly improved the quality of the regrowth. The waveguide etch and metal grating/waveguide integration were also redeveloped to be more supportive of the material platform and the integration of micro-scale and nano-scale features. Very little previous work had been done to use the tensile strained AlInGaAs QW structure to make grating lasers. While some future development is needed, significant progress was made to demonstrate the capabilities of integrating sub-wavelength metal gratings with in-plane laser cavities on this platform.

A distributed Bragg reflector (DBR) lasers with metal grating mirrors is demonstrated as a proof of concept. Maximum output power ranges from 10-14 μW

with differential efficiencies of 0.06-0.075%. The inefficiency of these lasers can mainly be attributed to losses incurred when the optical cavity mode contacts the metal gratings. Single mode lasing is demonstrated in DBR lasers with two matched metal grating mirrors. We show that sub-wavelength metal gratings can serve as integrated optical circuit elements, but without a major reduction in losses, they should only be used in cases where other mirror options are not valid design choices. The devices were designed with consideration given to likely applications areas where metal grating mirrors would be required. Near-term integration is demonstrated to be feasible for such applications.

7.2 Future Work

In the following sections, we will discuss some tangible steps that can be taken to advance the work presented in this dissertation.

7.2.1 Material Platform

One of the first suggestions moving forward with this work is to move away from the tensile-strained AlInGaAs quantum well platform. While this platform did provide some advantages, namely large amounts of TM gain, it presented far too many fabrication and performance challenges. Our suggestion would be to use a more well-tested, robust gain medium, such as bulk InGaAs. This gain medium should provide fewer issues with wet etching. It will also amplify both TE and TM polarization

making it a much more versatile platform choice[1] and it is significantly less expensive than our QW platform.

7.2.2 Fabrication Improvements

We believe that additional improvements could be made to device performance and reliability by making two main changes to the fabrication process unrelated to the material platform issues. First, the grating etch could be performed much more repeatably and with better sidewall profiles by switching from an MHA etch in RIE to a chlorine-based ICP etch for gratings[2]. This ICP etching technology currently exists at UCSB, but it was not available at the time these devices were fabricated. Additionally, designing and employing better test structures to accurately measure grating depth would be extremely helpful to the process.

The second improvement that could be made would be to carefully ensure better contact metal deposition. Poor contacts were the major limiting factor in the yield of these devices, and while this step is one of the most commonly performed, it has an enormous effect on device performance. Additional metal deposition or imaging would be a simple way of ensuring better device characterization.

7.2.3 Additional Device Integration

With the above improvements, there should be more flexibility in the design space for devices that integrate sub-wavelength metal gratings. We made significant progress towards our two initial motivations, using sub-wavelength metal gratings to generate

compact on-chip delay and developing in-plane metal laser mirrors, but there is still work to be done before either of these can be fully demonstrated. For on-chip compact delay, the fabrication methods developed should prove useful. One of the best test structures that could demonstrate this effect is a Mach-Zehnder interferometer (MZI) designed with a metal grating integrated in one arm and no delay in the other arm. MZIs are commonly used this way when delay is needed on-chip[3], so this would be a demonstrable and feasible way to determine the potential for further on-chip integration.

As for the exciting applications with metal-coated nano-cavity lasers, the logical first step is to attempt to integrate the gratings with progressively smaller laser cavities. The major challenges here will be achieving adequate large mirror reflectivites and integrating nano-scale and micro-scale fabrication techniques. Patterning both the grating and the cavity at the same time and using a staged etch process similar to that used to make deep ridge waveguides[4] could prove to be an elegant solution to this problem.

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