Data Converter Interleaving: Current Trends and Future Perspectives

Christian Schmidt, Hiroshi Yamazaki, Gregory Raybon, Peter Schvan, Erwan Pincemin, S. J. Ben Yoo, Daniel J. Blumenthal, Takayuki Mizuno, and Robert Elschner

Abstract

Future generations of optical networks will require optical interfaces that operate beyond 1 Tb/s to keep up with the exploding worldwide Internet data capacity. The data converters, digital-to-analog converter (DAC) and analog-to-digital converter (ADC), significantly define the signal bandwidth that can be transmitted or received with an electro-optic transceiver. The foreseen improvements of complementary metal oxide semiconductor (CMOS) data converters in upcoming CMOS technology nodes do not scale to the expected interface data rates for future communications systems. To address this bandwidth requirement, parallel data converter architectures (i.e., interleaved data converters) are an intriguing solution to enable performance beyond the limits imposed by continuing traditional CMOS approaches. In this article, we discuss the performance requirements for future data converters and provide an overview of the projected evolution of fiber optic networks and the limits imposed by CMOS-only data converters. Interleaved data converter architectures, in both the electrical and optical domains, are described and discussed. Finally, an outlook is given on the future development of next generation DAC and ADC architectures. This article is based on the presentations and discussions in the workshop "Super DACs and ADCs — To Interleave or Not to Interleave" at the Optical Networking and Communication Conference 2019.

Introduction

Modern applications such as cloud computing, 5G, and the Internet of Things drive the demand for higher data rates. Optical communications systems are the premier solution for providing energy-efficient high-speed data transport. The traffic growth ranges between 30 and 60 percent per year depending on the network segment. and worldwide cloud data center traffic capacity is expected to exceed 21 Zetabytes by 2021 [1]. Accordingly, the data rate per wavelength optical interface needs to scale to beyond 1 Tb/s in the future.

Continuous improvements in advanced modulation formats, forward error correction (FEC), and digital signal processing (DSP) have increased the data rate, which is expected to exceed 1 Tb/s, with aggregate fiber channel capacity exceeding 100 Tb/s. To achieve this, it is more efficient to increase the aggregate channel capacity due to linear scaling laws as opposed to pushing limits due to signal-to-noise ratio (SNR), which obey logarithmically scaling laws given by the Shannon limit.

The data converters employed in electro-optical transceivers — digital-to-analog converter (DAC) and analog-to-digital converter (ADC) — significantly define the signal bandwidth that can be transmitted or received. These converters today are fabricated in complementary metal oxide semiconductor (CMOS) technology to scale the bandwidth with power and cost efficiently. However, there is an upcoming limit in the future scalability of CMOS as the transistor nodes, today at 7 nm gate size, will have trouble meeting future optical interface data rates, even as nodes scale to 5 nm and 3 nm. To alleviate this scaling issue, designers look to parallel data converter architectures (i.e., interleaved data converters), an approach that enables performance beyond the limits of CMOS. Therefore, state-of-the-art CMOS technologies are used in addition to circuits in material alternatives to silicon, to scale the aggregate converter and channel bandwidth.

This article is structured as follows. First, the evolution of fiber optics networks is outlined. Then the current status and future needs of CMOS data converters are explained. Afterward, methods for electronic data converter interleaving as well as the incorporated challenges are explained and discussed. Furthermore, optically interleaved data converters are presented in the subsequent section. Finally, an outlook is given on the future development of DACs and ADCs.

The authors discuss the performance requirements for future data converters and provide an overview of the projected evolution of fiber optic networks and the limits imposed by CMOS-only data converters. Interleaved data converter architectures, in both the electrical and optical domains, are described and discussed. Finally, an outlook is given on the future development of next generation DAC and ADC architectures.

Current and Future Evolution of Fiber Optic Networks

Over the past 10 years, deployment of 100G coherent wavelength-division multiplexing (WDM) systems, based on 32 GBd dual-polarization quadrature phase shift keying (DP-QPSK), has increased exponentially to fill the capacity needs of the global fiber communications infrastructure.

Christian Schmidt and Robert Elschner are with the Fraunhofer Heinrich-Hertz-Institute; Hiroshi Yamazaki is with NTT Network Innovation Laboratories and NTT Device Technology Laboratories; Gregory Raybon is with Nokia Bell Labs; Peter Schvan is with Ciena Corporation; Erwan Pincemin is with Orange Labs; S.J. Ben Yoo is with the University of California; Daniel J. Blumenthal is with the University of California Santa Barbara; Takayuki Mizuno is with NTT Network Innovation Laboratories.

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High-speed CMOS data converters are essential components for coherent communications: they provide the conversion between the digital and analog domain and vice versa. Their performance has been increasing year by year since their introduction a decade ago.

Modulation format		QPSK	8-QAM	16-QAM	32-QAM	64-QAM	128-QAM	256-QAM
Bits per symbol		2	3	4	5	6	7	8
Required ENOB (DAC)		1		2		3		4
Required ENOB (ADC)		>3.8		>4.9		>5.7		>7
Line Rate in Gb/s	400	128	85	64	51	43	37	32
	800	256	171	128	102	85	73	64
	1600	512	341	256	205	171	146	128
	3200	1024	683	512	410	341	293	256
	10000	3200	2133	1600	1280	1067	914	800

Table 1. Symbol rates in GBd for different line rates and modulation formats.

More recently, deployment of 200G coherent WDM systems based on 32 GBd DP 16-level quadrature amplitude modulation (QAM) is making inroads in metro systems. This allows increasing spectral efficiency by a factor of two, while further decreasing the cost per bit. In 200G long-haul applications, >56 GBd DP-QPSK systems are currently being deployed.

For 400G, the Optical Internetworking Forum presented a multi-source agreement (MSA) based on 64 GBd DP-16-QAM called 400-ZR. The interoperable 400G transceivers address data center interconnections having 80 to 120 km transmission reach and use pluggable optic modules.

For ultra-long-haul systems, advanced modulation techniques like probabilistic/constellation shaping (PS/CS) enable systems to operate closer to the Shannon limit and to better adapt the data rate. For a given constellation and given data rate, PS/CS improves the SNR margin by ~1–2 dB at the expense of a moderate increase of the baud rate (e.g. 39 GBd with PS/CS instead of 32 GBd with standard 16-QAM). System and subsystem vendors are announcing the availability of ~90 GBd PS/CS transceivers (up to 800G) in the upcoming months.

Historically, the fast technical evolutions in fiber optics have been supported by continued progress in CMOS technology that supports data converters and DSP application-specific integrated circuits (ASICs). Ten years ago, at the beginning of the coherent era, data converters used 65 nm CMOS technology with sampling rates around 40–56 GS/s and bandwidths around 16 GHz. In subsequent CMOS technologies (i.e. 40 nm, 28 nm, and 16 nm), the sampling rates could be increased to 65 GS/s, 92 GS/s, and 128 GS/s, while reaching bandwidths of 19 GHz, 26 GHz, and 35 GHz, respectively. Up to now, the power consumption of pluggable silicon photonics WDM transceivers has been reduced to less than 10 W/100G. Photonic ICs have contributed to divide the cost of 100G by a factor of five in the last five years.

CMOS Data Converters: Current Status and Future Needs

High-speed CMOS data converters are essential components for coherent communications: they provide the conversion between the digital and analog domain and vice versa. Their performance has been increasing year by year since their introduction a decade ago.

The main parameters of data converters for communications applications are sampling rate, analog bandwidth, effective number of bits (ENOB), and power consumption. In CMOS data converters, the analog bandwidth and the ENOB are bottlenecks for increasing the data rate. Current high-speed 16 nm FinFET CMOS DACs and ADCs achieve sampling rates of up to 128 GS/s with analog bandwidths of around 35 GHz and 8 bit nominal resolution at an average ENOB of 5.5 bits [2]. Both DACs and ADCs are integrated with the DSP to avoid the data interface bottleneck; for example, an interface rate of 3.2 Tb/s is required between four 100 GS/s 8-bit data converters and the DSP.

Current high-speed DACs are based on segmented current-steering architectures [2, 3]. Their performance is mainly limited by a code-dependent output impedance, timing mismatches between individual current cells, and clock feedthrough. High-speed ADCs are usually based on pipelined, successive approximation registers or flash architectures. The front-end consists of time-interleaved multiple track-and-hold (T&H) circuits, which are driven by a multi-phase clock. The high-speed ADC performance is mainly limited by the bandwidth of the T&H circuit and timing mismatches between the sub-ADCs.

The most recent energy-efficient CMOS technology nodes have an improved performance for digital circuits. For mixed-signal circuits, such as DACs and ADCs, the analog CMOS performance defines the analog bandwidth in the end. The CMOS technology's analog performance is subject to a declining transistor's f_t and $f_{\max}$ as well as interconnect parasitics. Further improvement in analog performance of upcoming technology nodes is questionable. Correspondingly, it is improbable that analog bandwidths beyond 50 or 60 GHz can be achieved with CMOS only. Moreover, the development costs are increasing with every technology generation, mainly due to lithography mask costs. To further increase both the analog bandwidth and the sampling rate, bipolar CMOS (BiCMOS) technologies offer an attractive alternative if they can be integrated or interconnected with CMOS DSP through innovative techniques. Among these new technologies are silicon germanium or III/V semiconductors (e.g., indium phosphide) for which f_t and $f_{\max}$ values >1 THz have been demonstrated, as described in [3].

To support a certain symbol rate, data converters need to have a sampling rate greater than the symbol rate and an analog bandwidth preferably at least half of the symbol rate. In Table 1, the symbol rates corresponding to current and possible future line rates are listed for different modulation formats from QPSK to 256-QAM, together with the minimum required DAC and ADC ENOB. The calculation assumes polarization-multiplexed signals and 28 percent FEC and protocol overhead. The required DAC ENOB assumes NRZ signaling (no pulse shaping, no pre-emphasis), and the required ADC ENOB is taken from [4]. For today's 800G communication systems, symbol rates of >85 GBd are required using 64-QAM. Going to higher line rates (e.g., 1.6 Tb/s) requires symbol rates of at least 128 GBd using 256-QAM, which are conceivable with projected improvements in CMOS technology. However, according to [5], line rates of 10 Tb/s are necessary in the near future (as of 2024 demanding symbol rates >800 GBd), which are well beyond current technological capabilities and require interleaved data converter concepts.

Data Converter Interleaving: Methods and Challenges

In recent years, several new ideas have been investigated to circumvent the limitations of a given CMOS DAC technology. High-speed digital and mixed-signal circuits were fabricated using Indium Phosphide Double Heterojunction Bipolar Transistor (InP-DHBT) technology, which is capable of producing circuits with high f_t and f_{max} while also providing high breakdown voltage leading to large output swing circuits. For example, indium phosphide (InP)-based technology developed at the III-V Lab in France uses 0.7 ?m geometries and has achieved an ft, fmax, and BVceo of 400°GHz, 390 GHz, and 5 V, respectively [6]. Another technology at NTT uses 0.25 μm geometries and has an f_t, f_{max}, and BV_{ceo} of 460 GHz, 480 GHz, and >3.5 V, respectively. Fabrication in InP is generally limited by low yield due to defects and large geometries, and thus less complicated designs are implemented compared to CMOS. Nonetheless, very high-speed multiplexers, 3-bit DACs, and analog multiplexer (AMUX) designs have been demonstrated, such as digital multiplexing up to 212 Gb/s [6] and an AMUX >110 GHz [7].

Figure 1 shows reported research results of coherent optical transmission systems that have utilized high-speed InP or BiCMOS circuits in the transmitter. The dashed lines represent the maximum information rate (line rate) attainable for PM-QPSK, PM-16QAM, and PM-64QAM formats. The marker shapes represent the modulation format used, while the colors represent the different interleaving methods: InP MUX (red), InP AMUX (green), InP SPDAC (yellow), and commercial BiCMOS DAC (blue). The results demonstrate progress in speed and complexity starting back in 2009 with a 224 Gb/s (56 GBd) QPSK transmission system to the present day where systems with 1 Tb/s capacity based on 64-QAM and more complex InP circuits have been demonstrated. The figure plots the net rate on the vertical axis, which represents the data rate after FEC overhead is subtracted. The net rate is plotted vs. symbol rate, which has steadily increased over time. The dashed lines represent the maximum information rate (line rate) attainable for PM-QPSK, PM-16QAM, and PM-QPSK formats. In most of the experiments, the receiver consists of a high-speed commercially available digital storage

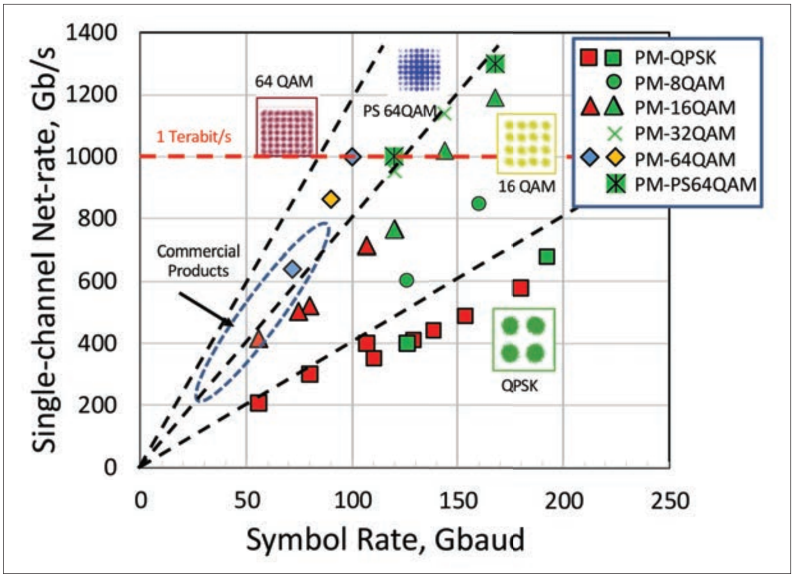

Figure 1. The net rate (data rate after FEC) vs. symbol rate for high symbol rate systems using high-speed circuits.

oscilloscope (DSO) that functions as the ADC and offline DSP. Consequently, the figure mainly represents progress in the transmitter technologies and reveals the need for high-speed ADCs for real-time systems. As a reference, the figure highlights commercially available products with CMOS technologies including real-time ADCs. Currently, commercial products have been announced that can achieve up to 800 Gb/s on a single channel. The figure shows the trends for QPSK, 16-QAM, and 64-QAM systems with a couple of demonstrations using 8-QAM and 32-QAM formats. Many of the references prior to 2019 can be found in [8].

The high-speed signals were generated with digital multiplexers (up to 180 GBd QPSK), digital multiplexers together with passive power combiners (up to 120 GBd 16-QAM), 3-bit selector InP-DHBT power-DACs (SPDACs, up to 90 GBd 64-QAM), analog-multiplexed DACs (up to 192 GBd QPSK [9], 160 GBd 8-QAM, and 1.30 Tb/s with PS-64-QAM), and frequency-interleaved DACs (up to 180 GBd QPSK).

In the following discussion, two of the most promising electrical interleaving concepts are covered: the analog multiplexing (AMUX) approach and the frequency interleaving (FI) approach based on mixers. Both approaches overcome the bandwidth constraint of CMOS data converters by virtually multiplying or dividing the analog bandwidth. A good overview on interleaved DACs can be found here [3]. As of today, these bandwidth-enhancing approaches are employed in commercial DSOs. However, they have not been integrated with CMOS data converters for communications products, either for DACs or for ADCs.

Analog Multiplexed DAC and Analog De-Multiplexed ADC

Figure 2 shows a conceptual block diagram of a coherent optical transmission system utilizing 2:1 AMUXs and 1:2 analog demultiplexers (ADMUXs). The transmitter and receiver each consists of a DSP and an analog front-end. Each

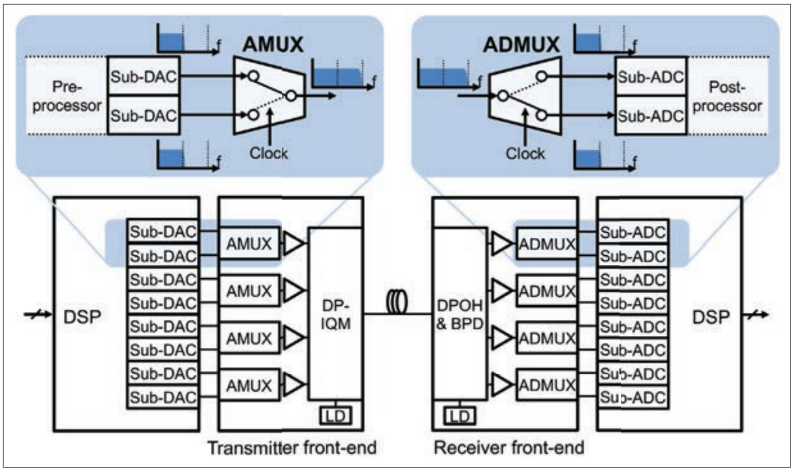

Figure 2. Block diagram of a coherent optical transmission system consisting of dual-polarization in-phase/quadrature modulators (DP-IQMs) and a dual-polarization optical hybrid (DPOH) with balanced photodetectors (BPDs), each supplied by a laser diode (LD). To enhance both the sampling rate and the analog bandwidth, the interleaved DACs and ADCs use AMUX and ADMUX, respectively.

DSP is integrated with eight sub-DACs/ADCs, and each front-end contains four AMUXs/ADMUXs. The other parts are the same as the standard coherent systems of today. On the transmitter side, each AMUX lets sub-signals from the two CMOS sub-DACs pass through alternately at the clock frequency. With a dedicated digital pre-processor, each subsystem consisting of two sub-DACs and an AMUX (hereafter called an AMUX-DAC) operates as a DAC with an analog bandwidth up to twice that of each CMOS sub-DAC [10]. Although the AMUX operates in the time domain, the function of the AMUX is equivalent to a superposition of the baseband components and the images of the two input sub-signals with specific relative phases and amplitudes in the frequency domain. Based on this frequency-domain interpretation, the pre-processor virtually weaves the targeted signal into two half-bandwidth digital sub-signals, which are converted to analog sub-signals by the sub-DACs and multiplexed by the AMUX to generate the targeted full-bandwidth analog signal. On the receiver side, each ADMUX-ADC operates vice versa: each ADMUX lets every second sample of the input signal pass through alternately at the clock frequency to one of the two CMOS sub-ADCs.

In order for the AMUX and ADMUX to provide analog bandwidths significantly exceeding that of the silicon CMOS converters, they need to be fabricated on compound platforms. State-of-the-art AMUX ICs with an analog bandwidth of >67 GHz [11] and > 110 GHz [7] have been fabricated in SiGe and InP HBT technology, respectively. To mitigate attenuation of the wideband analog electronic signals, it is preferable that the AMUX and the ADMUX are placed close to the optical modulator and the photodiode, respectively. An integrated optical transmitter front-end, in which AMUXs with integrated driver amplifiers are wire-bonded to an ultra-wideband optical IQ modulator (IQM), was fabricated and generated up to 192-GBaud signals [9]. The ADMUX-ADC has already been employed in commercial DSOs, but has not been demonstrated with CMOS ADCs or in an integrated optical receiver front-end yet. A similar architecture based on harmonic mixing has been employed in commercial DSOs as well.

The hardware configurations of the AMUX-DAC and ADMUX-ADC are completely symmetric with respect to the two sub-converters, which is favorable for balancing the two branches. The SNR of the combined converter is fundamentally limited by the ENOB of the individual data converters. Further, the nonlinearities of the AMUX's data path and the AMUX clock phase noise put an upper limit on the achievable SNR. Average SNR values of 15.7 dB have been achieved over 80 GHz bandwidth [10].

Frequency-Interleaved DACs and ADCs

For interleaving in the frequency domain, a broadband signal is split into multiple frequency bands, which are each individually converted between the digital and analog domains and vice versa, and finally recombined.

In Fig. 3, a conceptual block diagram for both a frequency-interleaved (FI)-DAC and an FI-ADC is visualized. For the FI-DAC, the broadband digital input signal is split into multiple frequency bands, which are each downconverted to baseband prior to digital/analog conversion. At the sub-DACs' outputs, the unnecessary hold spectra of the individual sub-signals are suppressed by analog low-pass filters. The filters for the lowest sub-signal are included in the multiplexer filter (MF). The sub-signals representing the different frequency bands of the signal are upconverted to their respective carrier frequency with analog radio frequency (RF) mixers or analog in-phase/quadrature (I/Q) mixers. Finally, the sub-signals are combined with the MF forming the desired continuous spectrum without gaps or guard bands. The MF's characteristics suppress both fed-through local oscillator (LO) signals and undesired mixer sidebands. Depending on the suppression ratio, residual spectral components may remain, reducing the SNR of neighboring frequency bands [3].

The FI-ADC operates in reverse of the above. The broadband analog input signal is split into multiple frequency bands with the MF. Analog mixers downconvert the sub-signals to baseband, which are then low-pass-filtered prior to digitizing with the sub-ADCs. In the DSP, the individual sub-signals are recombined to recover the broadband input signal of the FI-ADC. The FI-ADC concept has been employed in commercial DSOs, but has not been migrated to CMOS ADCs for real-time use. The FI-DAC concept has been demonstrated in multiple laboratory experiments during the last years [12,13] with commercial products yet to be released.

The FI concept is based on an asymmetric configuration, which exacerbates synchronization and compensation of analog impairments with DSP algorithms. The SNR performance of the combined data converter is fundamentally limited by the ENOB of the individual data converters. Further, the analog mixer's nonlinearities and the LO's phase noise put an upper limit on the achievable SNR. The critical component for scaling the concept to more frequency bands is the MF with a sufficiently high port count, which is preferably realized with a high-insertion-loss

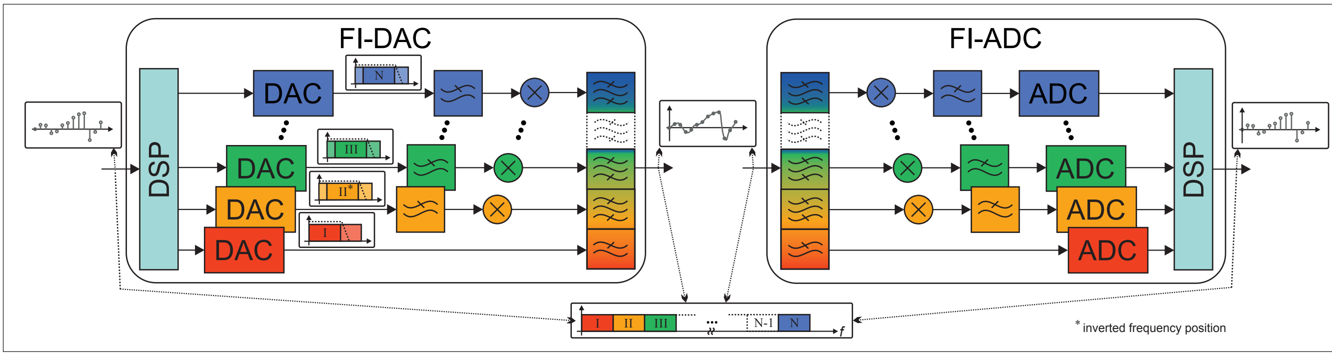

Figure 3. Conceptual block diagram of the frequency-interleaved DAC (FI-DAC) and the FI-ADC, each based on an analog processing system consisting of mixers and filters.

cascade of diplexers. Moreover, integration of the MF's filter structures in CMOS technologies is highly challenging nowadays. Further, the parameters of the FI data converter are interdependent, resulting in a limited variability in terms of bandwidth and sampling rate in the end [3].

Optical Data Converter Interleaving

For ultra-high-speed signal generation and detection, purely electrical concepts will finally be insufficient. From a modern perspective, electrical circuits with analog bandwidths up to 500 GHz are conceivable in advanced technologies such as InP in the future. However, electronics' analog bandwidth will eventually be limited by the electron mobility in the respective material, which can only be overcome by optical interleaving concepts.

In optical communication systems, Nyquist WDM is commonly used to transmit multiple nearly-rectangular-shaped spectral bands closely packed with minimal guard bands. However, the wavelength grid allows for multiple parallel signals rather than a single, free-defined broadband signal, which is required for the vision of truly elastic optical networks (EONs) with flexible spectrum assignments, flexible modulation formats, and a flexible grid.

Such a broadband signal can be generated using an optical frequency comb with the guard bands between the channels reduced to zero [14], which is visualized in Fig. 4.

For optical arbitrary waveform generation (OAWG), the input signal is split into multiple frequency bands in the DSP unit. Each frequency band is then modulated onto a certain wavelength of an optical frequency comb with a dual-polarization IQ modulator (DP-IQ-MOD). The optical frequency bands are seamlessly combined with an arrayed waveguide grating (AWG) to a combined freely defined waveform.

For optical arbitrary waveform measurement (OAWM), the broadband input signal is split with an AWG into multiple optical frequency bands. Parallel DP coherent receiver front-ends (COH-RX-FE) convert each frequency band to the electrical domain, in which the corresponding signal is then digitized with four ADCs each. A joint DSP recombines the broadband signal.

For practical OAWG and OAWM implementations, large-scale photonic integrated circuits should stably integrate various photonic components on a single platform, preferably co-integrated with electronics [15]. This large-scale photonics integration ensures phase stability between the frequency bands. Recent advances in silicon photonics support high-yield fabrication of OAWG and OAWM with discrete electronic ICs to be flip-chip bonded on them. One advantage of OAWG and OAWM is that it can be nearly free of systematic degradation of ENOB when scaling to high sampling rate (e.g., TS/s) utilizing many low-sampling-rate electronics as long as a low-jitter optical frequency comb is utilized. For instance, 1 THz 10-bit ENOB OAWG and OAWM can be achieved utilizing 100 10 GHz 10-bit ENOB ADCs and DACs if an optical frequency comb (OFC) with an RMS jitter of < 0.36 fs is available (e.g., carrier-envelope-stabilized OFCs), while standard OFCs with ~40 fs RMS jitter (e.g. with commercial mode-locked lasers or micro-resonators) will support ~4-bit ENOB at 1 THz. Achieving similar scaling to such high bandwidth at high ENOB (1 THz 10-bit ENOB) with electronic data converters alone is considered currently not possible due to higher electronic noise and jitter values [15]. Note that an optical super-channel with multiple closely spaced optical channels could be used instead to prevent the comb-induced ENOB penalty; however, the resulting signal is not arbitrary as for OAWG.

Comparison of Concepts and Outlook

Electrical interleaving enables the bandwidth constraint of CMOS data converters to be overcome up to a certain limit. The AMUX/ADMUX concept has a symmetric and filter-less configuration, which can be well integrated with existing IC manufacturing technologies. The FI approach with asymmetric signal paths requires bulky RF microwave multiplexer filters to combine or to split the broadband signal. These filters can hardly be integrated with existing technologies as of today. However, high-frequency mixers are already available for frequencies up to 300 GHz. For both concepts, DSP is required: for the AMUX/ADMUX, the main challenge is the overlapping spectra. For the AMUX, they cover the whole output bandwidth and need to be calculated accordingly. The ADMUX essentially downsamples the input signal: its outputs are subject to aliasing effects, which are corrected in the DSP. For the FI approach, the main challenges are the asymmetrical signal paths and the mixers' nonlinear distortions. Thus, the multiplexer filter can be principally omitted, resulting in a more complex DSP and higher loss-

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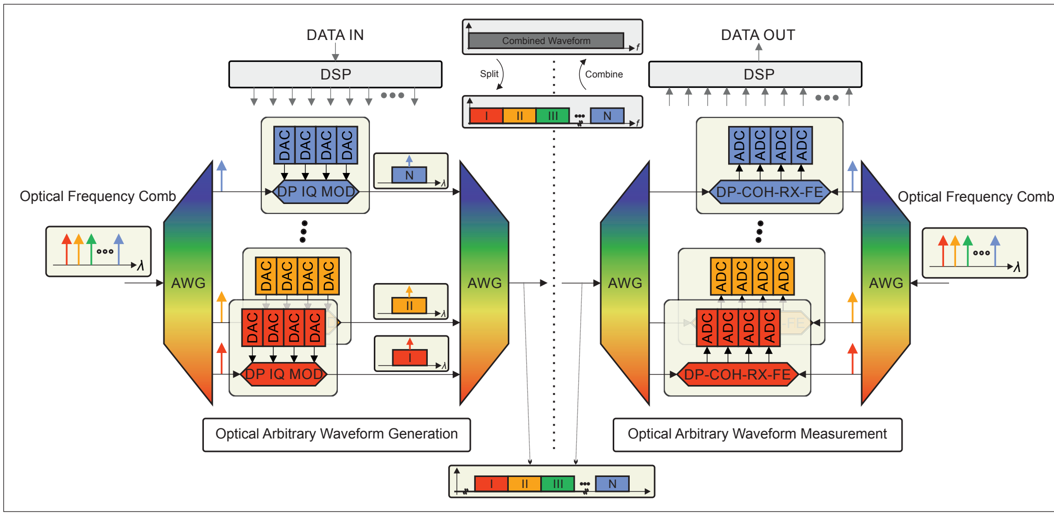

Figure 4. Block diagram of optical arbitrary waveform generation (OAWG) and optical arbitrary waveform measurement (OAWM).

	AMUX-DAC/ADMUX-ADC	FI-DAC/FI-ADC	OAWM/OAWG
Bandwidth	Determined by DACs and A(D)MUX	Determined by DACs, mixers and combiner	Covers the entire optical fiber transparency bandwidth
Jitter	A(D)MUX clock jitter dominates DAC clock jitter impairments	LO dominates DAC clock jitter impairments	low-jitter optical frequency comb required
Scalability	Higher A(D)MUX order	More mixers and filters; combiner with more ports	Limited by DSP complexity
Integration	Feasible	Filters are challenging	Feasible with recent silicon photonics integration and packaging technologies

Table 2. Comparison of interleaving concepts.

es for high-bandwidth-capable passive combining along with an ENOB loss. Both approaches can be scaled to higher interleaving orders. However, as more signal paths are connected to a circuit node, the parasitic capacitances rise, putting an inherent limit on the number of paths.

The power consumption of a single data converter is twice as high if it operates at twice the speed. By using *N* interleaved data converters, which increase the sampling rate *N*-fold, the additional power consumption for interleaving originates in the analog components, that is, AMUX/ADMUX, clock generation, amplifiers, and so on, and the more advanced DSP. In terms of integration, the AMUX/ADMUX is more suitable for communications products, whereas the bandwidth potential of the FI approach and its bulky filters will enable broadband test and measurement applications. Due to the need for high data rates the interleaved data converters may soon be deployed in all network segments.

The optical interleaving extends existing WDM ideas to provide a scalable concept enabling quasi-unlimited optical bandwidth in the end. Major challenges are a low-jitter OFC, the integration of many optical components enabling phase stability between the individual frequency bands, and a DSP architecture handling the splitting and the combining of many sub-signals. Efforts toward a distributed DSP architecture for this concept are essential. Optical interleaving could be included into every transceiver, at least for a subset of wavelengths. The power consumption is equivalent to that of a current WDM system plus additional power for the more complex DSP.

It is foreseen that electrical interleaving will be pursued for the next couple of years to enable broad-bandwidth single-wavelength transceivers. Later, optical interleaving will complement the electrical approach, rather than substitute it, to enable truly fully flexible optical networks.

Conclusion

The demand for high data rates rises continually in all network segments, but the bandwidth of energy-efficient CMOS data converters does not scale accordingly. Interleaved data converter architectures in both the electrical and optical domains are a potential path to bridge the emerging gaps and push fiber capacity. Electrical interleaving will be pursued in the next couple of years, enabling broad-bandwidth single-wavelength transceivers. Later, optical interleaving will complement the electrical approach, allowing waveforms spanning multiple terahertz of bandwidth, which enable truly flexible optical networks.

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Biographies

Christian Schmidt (christian.schmidt@hhi.fraunhofer.de) received his B.Sc., M.Sc., and Dr.-Ing. (Ph.D.) from Kiel University, Germany, from Karlsruhe Institute of Technology, Germany, and from Technische Universität Berlin, Germany, respectively. Since 2015, he has been with the Fraunhofer Heinrich-Hertz-Institute, Berlin, Germany. His current research interests include broadband signal generation for next generation optical communications networks.

Hiroshi Yamazaki (yamazaki.hiroshi@lab.ntt.co.jp) received his M.S. degree in human and environmental studies from Kyoto University, Japan, in 2005, and his Dr. Eng. degree in electronics and applied physics from Tokyo Institute of Technology, Japan, in 2015. In 2005, he joined NTT Photonics Laboratories. He is concurrently with NTT Network Innovation Laboratories and NTT Device Technology Laboratories, Kanagawa, Japan, where he is involved in research on devices and systems for high-speed optical transmission.

Gregory Raybon [F] (gregory.raybon@nokia-bell-labs.com) is a Distinguished Member of Technical Staff at Nokia Bell Laboratories, Holmdel New Jersey. He received his B.S. degree in electrical engineering from Penn State University in 1984 and his M.S. degree in material science from Stevens Institute of Technology in 1989. He is a Fellow of OSA.

Peter Schvan (pschvan@ciena.com) received his M.S. in Physics and his Ph. D. in Electronics in 1985. After joining Nortel he has worked on device modeling, technology development followed by circuit design for fiber optic communication. Currently he is director of analog design at Ciena, Ottawa, involved in the development of broadband amplifiers, high speed A/D and D/A converters. He gave several workshop presentations and authored or co-authored over 40 publications.

Erwan Pincemin (erwan.pincemin@orange.com) graduated from Ecole Supérieure d'Optique, Orsay, France, and from Université Paris XI, Orsay, France, in optics and photonics, both in 1996. He currently works in Orange Labs, Lannion, France, where he is in charge of research on 100 Gb/s and beyond optical transmission, advanced modulation formats, coherent detection, digital mitigation of fiber impairments, flexible optical networking, and quantum communications. He is an author and co-author of more than 140 journal and conference papers and 28 patents.

S. J. Ben Yoo [F] (sbyoo@ucdavis.edu) received his B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, California, in 1984, 1986, and 1991, respectively. He currently serves as a Distinguished Professor of electrical engineering at the University of California Davis. His research includes 2D/3D electronic/photonic integration for future computing, communication, imaging, navigation systems, and the future Internet. Prior to joining UC Davis in 1999, he was a senior research scientist at Bellcore. He is a fellow of OSA.

Daniel J Blumenthal [F] (danb@ucsb.edu) received his Ph.D. degree from the University of Colorado, Boulder (1993), his M.S.E.E. from Columbia University (1988), and his B.S.E.E from the University of Rochester (1981). He is a professor in the Department of ECE at UC Santa Barbara and director of the Terabit Optical Ethernet Center (TOEC), and heads the Optical Communications and Photonics Integration (OCPI) group. He has published over 425 papers. Heis a Fellow of the National Academy of Inventors (NAI) and the Optical Society of America.

Takayuki Mizuno (takayuki.mizuno.zp@hco.ntt.co.jp) received his B.E. degree in applied physics, his M.E. degree in crystalline materials science, and his Dr. Eng. degree in quantum engineering, all from Nagoya University. In 2000, he joined NTT Corporation. Since 2013, he has been managing research on ultra-high-capacity optical transmission systems at NTT Network Innovation Laboratories. He is currently serving on the Technical Program Committee of the Optical Fiber Communication Conference.

Robert Elschner (robert.elschner@hhi.fraunhofer.de) received his Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Technische Universität Berlin, Germany, in 2006 and 2011, respectively. In 2005, he was with Telecom ParisTech. Since 2010, he has been a member of the scientific staff and project manager at Fraunhofer Heinrich-Hertz-Institute, working in the field of digital coherent optical transmission technology. He is currently serving on the Technical Program Committee of the Optical Fiber Communications Conference.

Electrical interleaving will be pursued in the next couple of years enabling broad-bandwidth single-wavelength transceivers. Later, optical interleaving will complement the electrical approach allowing waveforms spanning multiple Terahertz of bandwidth, which enable truly flexible optical networks.