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Frequency-Stabilized Links for Coherent WDM Fiber Interconnects in the Datacenter

(Invited Paper)

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***Abstract*— The continued growth in Hyperscale data center (HDC) deployment is expected to drive world-wide Internet traffic to an astounding 21 zettabytes by 2021. This growth will place increased demands on data center interconnects (DCIs) and drive the capacity of the underlying electronic application specific integrated circuit (ASIC) switch chips that route DCI ethernet traffic, from 12.8 Tbps per chip today to 100 Tbps and beyond in the future. This astounding growth will push the limits of today's incoherent fiber link technologies that connect switches, including power dissipation, density, and practical engineering solutions. To overcome these limits, high capacity coherent WDM, traditionally relegated to the metro and long-haul networks, will need to move into the DCI. However, migrating coherent WDM into the DCI, particularly for link distances less than 2 km, will require elimination of power consuming and costly technologies like the digital signal processor (DSP). Additionally, new photonic integration technologies will be needed to co-locate the coherent optical interfaces directly with switch ASICs to alleviate the bandwidth, power and density limits. In this paper, we introduce a new approach to DSP-free coherent WDM for the DCI called FRESCO: FREquency Stabilized Coherent Optical Links for Low Energy DCIs. FRESCO utilizes spectrally pure, ultra-stable light source technology, normally associated with high-end scientific applications like atomic clocks, to enable high capacity high-order WDM QAM with low bandwidth, low power electronics normally associated with RF links. Terabits per second FRESCO links based on shared, stabilized sources and high-density coherent WDM silicon photonic coherent transceivers that are co-located with the switch ASIC will pave the way to a DSP-free coherent WDM scalable DCI solution.**

***Index Terms* — Optical fiber communication, optical interconnections, optical modulation, photonic integrated circuits, silicon photonics, frequency locked loops, phase locked loops, laser noise, noise cancellation, phase noise, wavelength division multiplexing.**

I. INTRODUCTION

Hyperscale data centers are expected to support 21 Zettabytes per year and represent over 50% of share of installed data center base in 2021 [1]. As these data centers become prevalent, demand for increased capacity of electronic switch ASIC chips, the routing engines of the Data Center Interconnect (DCI), will grow from 12.8 Tbps today to next generation 25.6 Tbps, pushing capacity demands and straining energy resources [1, 2]. It is now expected that the switch ASIC capacity will grow to an astounding 100 Tbps and higher pushing today's engineering limits. As illustrated in Figure 1, the scale of this challenge is equivalent to integrating onto a single electronic chip package, the electronic switching and interface subsystems (buffering, switching, scheduling, etc.) of the 92 Tbps Cisco CRS-1 and CRS-3 [3] that occupied up to 72 interface/buffer equipment racks and 8 switch equipment racks.

The capacity of these packet routing systems was limited in large part by the "power spreading problem" [4], a practical set of design constraints where increases in on-chip capacity leads to the chip exceeding the allowable power dissipation per area (e.g. 100 Watts per cm^2). Yet this use of multiple chips requires added electronic transceivers that can drive traces and possibly regenerators and re-timers on the traces, further exacerbating the power consumption scaling by adding a communication power tax.

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As the practical line-card power envelope (power per area) is exceeded, multiple line-cards or boxes must be organized into a shelf and then into multiple racks. Each time chips are moved farther away to accommodate capacity driving power limits, by spreading these increasingly higher capacity chips over line-cards, shelves, boxes and racks, a continued increase in communications power overhead occurs, hence the power spreading problem. As high speed data is moved between racks and systems, optical fiber links are employed. Today, the optical interfaces in a DCI utilize relatively simple incoherent on-off modulation, parallel fibers based transceivers located in pluggable modules, an approach that will run in serious constraints related to the power spreading problem as the systems scale. For example, a 102.4 Tbps switch with 100G electrical interfaces will need 1024 bidirectional SERDES, and hence in excess of 2048 fibers. The power consumption and alignment tolerances posed at these scales is a serious concern. Using approaches deployed in today's metro links like dense wavelength division multiplexing (DWDM) of NRZ/PAM-4[5] is a possible approach, however the complexity and power consumption of PAM-4 circuitry to gain a factor of 2 in spectral efficiency will limit the capacity scaling of this technology. New solutions will be needed to address scaling barriers including moving the optics closer to the switch ASIC[6-8] and spectrally efficient, high capacity fiber modulation[9, 10] techniques.

In this paper we describe an approach to bring co-packaged, co-located, high capacity coherent optical WDM into the DCI through high degree of photonic integration and operation in a new regime of optical frequency stability. Our approach, the ARPA-e OPEN funded FRESCO: **FR**equency **S**tabilized **C**oherent **O**ptical WDM links for energy efficient DCIs, is designed to provide a power envelope and chip/fiber-count complexity that scales the switch ASIC optical I/O to 100 Tbps and beyond. We propose utilizing ultra-high frequency stability to bring coherent WDM into the DCI without the high cost, large footprint and power consuming technologies associated with traditional coherent WDM systems including digital signal processors (DSPs) and high bandwidth analog and high speed digital electronics [11, 12] as well as employing highly integrated co-packaged switch/optics [6, 8].

II. Moore's Law of Networking

Today, the equivalent of racks of electronic equipment in the early 2000s is now integrated into single switch ASIC chips. A typical data center is built in layers starting at the top of the rack (TOR) switch that is used to connect multiple servers (e.g. 40) within a rack, to other racks connected through an intra-DCI and to other data centers via inter-DCIs. The switch ASIC chip is responsible for routing packets over optical fibers using pluggable fiber optic modules located on the front face plate of a switch box. The capacity evolution of the switch ASIC chip has scaled dramatically, from 2.0 Tbps to 12.8 Tbps in 2017/2018 with announcement of tapeout for 25.6 Tbps switches in 2020/2021 (Figure 2).

An example switch box is the Barefoot Newport 12.8T based on the Barefoot TOFINO 2 switch ASIC (Figure 3). Massive arrays of parallel traces on the circuit card carry high speed data from between the switch ASIC and optical transceivers operating at 400 Gbps each (4 fibers in each direction, 100 Gbps per fiber), with 32 modules required to support the switch capacity. This standard configuration requires cooling for the switch ASIC and other electronics as well as the 400 Gbps transceivers, today at about 8-10W each, leading to a faceplate power density of up to 320 W. These power considerations show that as the switch ASIC capacity and power dissipation are increased, the optical interconnect density and power will push what is known as faceplate and power envelope limits.

One challenge to integrating a system like the CRS at the chip-scale, including 100 Tbps of switching, buffering and other electronic functions, is limits equivalent to a Moore's law for networking (Figure 4a). To reach capacities of 102.4 Tbps and beyond, the transistor speed and node size must continue to decrease. However, at these speeds the chip power efficiency does not remain flat with increased density. For example, a 12.8 Tbps switch housed on a 25 mm x 25 mm die (Figure 4b) utilizes 7 nm transistor node technology to support switch functions as well as 256 lanes of electrical I/O transceivers at the perimeter, each operating at 50G PAM-4. If the node size is decreased to 5 nm transistor technology, a 1.8 increase in transistor density can be realized but with only a 20% power reduction. Looking towards continuing growth to 102.4 Tbps switch ASICs, this scaling behavior is dominated by the power spreading problem for networking. Additionally, this does not include the optical pluggable transceivers that today are located remotely from the ASIC, further driving up power consuming on-chip I/O drivers, on-board regenerators and pluggable optics.

Historically, the optical I/O capacity, density and power efficiency lags behind that of the switch electronics. Data on the switch chip is communicated via on-chip electrical transceivers connected to high speed electrical busses on a circuit card or interposer that in-turn are connected to fiber optic pluggable transponders located on a faceplate located multiple centimeters away. The chip electrical transceivers are scaled using traditional data serializers/deserializers (SERDES) that bring the native switch ASIC bus rate up (e.g. 1 GHz) to an off-chip modulation rate (e.g. 100 Gbps) using non-return-to-zero

(NRZ). New generation electrical transceivers also support multi-level PAM-4 modulation to increase the I/O bit-rate while maintaining single die form factor and 256 I/O pinout. As higher rate electrical transceivers are employed, periodic high-speed re-timer chips are required between the switch and pluggable optics. Today, the optical modules are connected to the DCI via parallel spatial division multiplexing (SDM) fibers communicating with NRZ binary on-off modulation (e.g. 100 Gbps per fiber x 4 fibers). A possible next step is to move the fiber to multi-level PAM-4, used in longer metro-area links, to provide a factor of 2x in capacity. However, PAM-4 has a strict signal to noise (SNR) requirement that increases cost and electronics complexity. Moving to PAM-8 and higher multi-level formats is impractical due to these SNR limitations as well as signal distortion, circuit complexity and the need to increase the laser output power and lower relative intensity noise (RIN).

Deployed 50 Gbps NRZ SERDES switches incorporate electrical transceivers that communicate with faceplate mounted optical modules operating at 50 Gbps over each of 4-fiber transmit (Tx) and 4-fiber receive (Rx) for an aggregate 200 Gbps send and receive. Today, new generation 12.8 Tbps switch can operate with a 2x increase in SERDES rate (100 Gbps NRZ) or maintain 50 Gbps with PAM-4 modulation (100 Gbps PAM-4), each requiring 32 x 400 Gbps modules over 4-fiber Tx and 4-fiber Rx. The number of modules and Tx and Rx fibers for 100Gbps PAM-4 to support 102.4 T switches is 256 modules and 2048 send and receive fibers (Figure 5). Contemplating 800 Gbps pluggable transceivers, the power dissipation of 128 faceplate pluggable modules and practical issues supporting 1024 Tx and Rx fibers will lead to extremely dense connectors and 2.56 kW at the faceplate (assuming 20 Watts per module). These factors push power and engineering limits and lead to a move away from pluggable optics.

The switch ASIC chip and optical I/O power consumption can be estimated as the capacity scales from 12.8 to 102.4 Tbps. An estimate of the switch power (red curve) based on CMOS scaling laws is shown in Figure 6. The optical I/O curves (black, yellow, blue) are the sum of the switch power and the estimated optical I/O for traditional NRZ SERDES, PAM-4 and a co-packaged FRESCO approach (described in this paper). The optical interface power should remain flat and track that of the switch ASIC power. The shaded regions indicate where the power envelope tracks the switch, with NRZ SERDES and PAM-4 diverging from the switch as the capacity approaches 25.6 Tbps and new solutions required at higher than 51.2 Tbps. While we focus in this paper on a frequency-stabilized coherent WDM solution, other viable options to be considered include co-packaged high channel count dense wavelength division multiplexing (DWDM) using for example PAM-4 or NRZ SERDES modulation with hundreds of wavelengths and multiple fibers. There will be energy and packaging tradeoffs between all these approaches, and heavy use of DWDM will require precision wavelength registration of all components as well as reliability and deployment issues associated with large fiber counts. In the end all approaches will have pros and cons related to details of a manufacturable, deployed solution, and in this paper we describe on approach that uses frequency stabilization, moderate wavelength count, and relatively moderate channel modulation bandwidths and high QAM modulation.

III. Coherent Optical in the DCI

As switches scale to 102.4 Tbps solutions, bringing coherent WDM optical links [10], traditionally used for metro- and long-haul fiber transmission [13], into the DCI is a potential solution. However, doing so requires eliminating power consuming and costly electronics like the digital signal processor (DSP) [10, 14] used in digital intradyne coherent systems [15, 16] or high frequency analog and digital electronics used in analog optical phase locked loop (OPLL) or electronic phase locked loop (EPLL) approaches [10, 11]. Intradyne detection and DSP processing, where the LO laser is free-running, was developed to overcome limits associated with imperfect lasers and analog PLLs (OPLL, EPLL). The power consumption and complexity of digital and traditional analog carrier and phase recovery increases with bit rate and channel capacity. Today, a 400 Gbps coherent DSP enabled transceiver can consume between 15 W – 20 W and scaling this approach to connect 100 Tbps switch ASICs faces power envelope, footprint and engineering limits.

A typical DSP-based digital optical coherent transmission system with transmitter and receiver DSPs [17] is illustrated in Figure 7. At the transmitter, parallel data streams are converted into symbols that are pulse shaped, equalized and amplified to generate in-phase and quadrature electronic drive signals (one for each polarization state) applied to an optical IQ modulator. The IQ modulator impresses baud-rate in-phase and quadrature modulated symbols on an appropriately chosen linewidth transmit laser. At the receiver, the received optical signal is mixed with a free-running LO laser through an optical hybrid and converted with differential photodetectors. All frequency and phase information of the transmitted signal is available at the differential detector outputs [14]. Sampling the detected in-phase and quadrature components with fast analog to digital converters (ADCs) returns a constellation that freely rotates due to the random carrier relative frequency drift and stability between the Tx and LO lasers. A frequency tracking algorithm is employed in the DSP to digitally compensate for this random intermediate frequency (IF) offset. After frequency offset correction, the recovered constellation has random rotational noise (phase jitter) due to beating of the phase noise (linewidth) of the independent Tx and LO lasers and other phase noise sources in the system (e.g. optical fiber). Sophisticated real-time phase error estimation and cancellation techniques are employed to remove the laser and fiber phase noise and recover the transmitted in-phase and quadrature components that are then converted using multi-level I and Q bit-slicers to recover the transmitted symbols and symbol to bit-mapping to return the transmitted data.

The requisite laser linewidth, a key parameter for coherent communication, is set by the following: modulation format, baud rate and bit error rate (BER) as well as the type of digital

or analog carrier and phase processing used, channel SNR and other impairments.

The laser linewidth, a measure of the phase (frequency) noise, and its dependence on the bit rate (baud rate) and required BER is determined by the received SNR and residual phase error after digital phase recovery or phase. For example, in a 16-QAM modulated system with 1E-3 BER the linewidth to baud rate ratio is ~ 1E-4 [18] and for 64-QAM using digital carrier phase estimation the ratio is on the order of 3E-8 e.g.,1.2 kHz at 40 Gbps [19] while for higher order QAM where low data rates are modulated onto each of multiple parallel subcarriers on each wavelength, a more relaxed linewidth requirement at 73 Msps leads to a ratio of 1.9E-4 e.g., a linewidth of 10s of kHz [20]. Pushing to ultra-high QAM, record coherent transmission utilized a 1.5 μm wavelength acetylene (C_2H_2) frequency stabilized fiber laser with a 4 kHz linewidth with receiver analog OPLL for 3 Gbaud 1024-QAM [21] and 2048-QAM [22] transmission. With analog phase and frequency tracking systems that employ OPLL, the required bandwidth is inversely proportional to the laser phase noise and therefore proportional to the bit rate, making it difficult to scale this systems to high capacity and low power consumption. Additionally, OPLL requires circuits with highly integrated feedback loops and feedback delays that can compensate for laser phase noise [23]. More recently, 3 Gbaud 4096-QAM fiber transmission was demonstrated using intradyne detection, DSP carrier and phase recovery, probabilistic shaping and ultra-narrow instantaneous (Lorentzian) linewidth (1 Hz) box-sized Tx and receive LO lasers [24].

The digital or analog processing bandwidth and power consumption for coherent carrier and phase recovery at the receiver is related to the frequency (phase) noise and carrier stability of the Tx and LO lasers. For high performance coherent systems, the generic full-width-half-maximum (FWHM) laser linewidth definition provides limited information of the required frequency (phase) noise. The fundamental, or instantaneous linewidth [25], provides high frequency (far-from-carrier) noise but does not contain important close-to-carrier noise components that can determine lineshape and the fractional frequency stability (carrier jitter) as well as the longer term carrier drift (stability). To fully understand the relationship between power consumption and circuit complexity for carrier and phase recovery, detailed optical frequency and phase noise as well as the fundamental and integral linewidth [26] [27] and frequency stability [28] must be employed.

Phase and frequency noise statistics of the laser emission, measured as spectral power in the single sideband (SSB) frequency offset from the optical carrier (ω_0), are quantified by power laws that describe physical noise sources (**Error! Reference source not found.**a). The Tx and LO laser phase (frequency noise) statistics will determine the constellation and recovered symbol SNR after frequency tracking in Figure 7.

The laser phase noise is measured in spectral energy of random phase shift per unit frequency (rad^2/Hz) and the frequency noise measured in spectral energy of random frequency changes from carrier per unit frequency (Hz^2/Hz). As illustrated in Figure 8a, noise spectra are calculated from the same measurements with phase noise plotted as the frequency noise normalized to the relative frequency (ν^2). The white frequency noise (WFN) regime, also called far-from-carrier noise, defines the fundamental (Lorentzian) component of the laser linewidth. The $1/\nu$ close-to-carrier noise contributes to random frequency components near the carrier and is often a limiting factor to the linewidth and carrier fractional stability (Flicker FM) while long term drift determines frequency stability. Other power law noise contributions can be considered and modeled in addition to $1/\nu$ noise.

The carrier stability of the Tx and LO lasers contributes to the constellation rotation shown in Figure 7, and will determine the movement of the IF which must stay within the transmission bandwidth for intradyne detection. The laser stability can be quantified in terms of the variance of the frequency deviation, relative to the carrier over different observation intervals, resulting in the well-known Allan Deviation (ADEV) measure [29]. A typical ADEV (Sigma Tau Diagram) is shown in Figure 8b, where subsequent measurements of the root of the fractional frequency noise variance ($\sigma_y(\tau)$) over short time observation intervals (small τ), expose the far-from-carrier white noise.

As time between measurement intervals (window) increases in Figure 8b, there is a flat portion (τ^0) where the carrier rms deviation is minimum, and over this interval a maximum stability, or fractional frequency noise (FFN) can be determined over that measurement interval. As the measurement interval increases, the long term drift of the laser carrier frequency can be quantified. These noise terms (phase/frequency) and drift contribute to the constellation point noise (spread) and rotation as shown in Figure 7, and is quantified by an error vector magnitude (EVM) of individual constellation points, and a rate of constellation rotation related to the carrier frequency drift.

Once the phase (frequency) noise power spectrum has been measured, linewidth calculations can be performed based on any of several definitions, each providing different application dependent meaning of the linewidth. Two commonly used definitions are the $1/\pi$ integration [27] (Figure 9a) and the β-separation line (Figure 9b). The former defined as effective frequency where the SSB phase noise area integrated from high frequency towards low frequency is $1/\pi$ rad^2 and the latter defined as the area under the frequency noise that sits below the β-separation line defined by $8\ln(2)f/\pi^2$. As the number of symbols and the symbol rate are increased, the performance, power consumption and complexity of the WDM coherent link must be defined in terms of the full laser frequency (phase) noise power spectrum and more complex metrics.

The challenge to bringing coherent WDM into the DCI requires alternate approaches to DSP intradyne and high frequency OPLL and EPLL heterodyne/homodyne. Opportunities for shorter reach DCI applications include removing DSP processing functions like chromatic dispersion (CD) compensation and reduce the complexity of error

correction algorithms required for longer distance transmission. High speed analog mixers and digital logic required for OPLL and EPLL phase and frequency lock, tied to wide bandwidth phase noise and laser stability consume high power and DSPs, OPLLs and EPLLs run into power and complexity issues as the bit rate per wavelength and number of wavelength increases. Other power consuming components include the Tx digital to analog converters (DACs) that map symbols to the IQ modulator drive voltages, the receiver ADCs that convert the optically demodulated I and Q waveforms to digital signals, high-speed digital slicers to return the transmitted symbols, clock and data recovery (CDR) circuits, and polarization controlling optics if dual polarization is used. There is an opportunity to eliminate the DSP carrier and phase recovery functions and low power DSP-free OPLL and EPLL solutions have been proposed [11], however, the power consumption will be difficult to scale to 100 Tbps. Recent demonstrations of DSP-free 400 Gbps single wavelength coherent for the DCI demonstrated a > 70% power savings in carrier and phase recovery using a self-homodyne coherent analog system where modulated signal and optical carrier are transmitted in separate fibers [12]. Solutions like this are an important step forward, but clear paths to supporting scalable DSP-free high order QAM multi-Tbps WDM links are needed.

IV. Frequency Stabilization and the FRESCO Architecture

Ultra-narrow linewidth, ultra-stable lasers, have served as the workhorse for precision scientific experiments including atomic clocks [30], atomic and quantum sensing [31, 32], and LIGO gravitational wave detection [33], yet these lasers occupy laboratory sized tables and equipment racks. Such systems provide an optical fractional frequency stability of better than 10^{-16} at 1 to 100 s and linewidths less than 40 mHz at 1550 nm [34]. Photonic integration of these ultra-stable spectrally pure sources opens the possibility to architect efficient high-capacity coherent fiber communications systems and new architectures. Recent progress towards integration include a sub-Hz fundamental linewidth stimulated Brillouin scattering (SBS) laser realized in a silicon nitride (Si3N4) waveguide platform [35] and a 30 Hz integral linewidth laser with $7x10^{-13}$ stability at 20 ms realized by locking to a 1 Billion Q optical reference μ-cavity [36]. Laser stabilization and linewidth reduction using an optical reference cavity can be achieved using energy efficient, low complexity, low-bandwidth control loops like the Pound-Drever-Hall (PDH) [5]. Due to the narrow optical resonance linewidth and stability of these extremely high-Q optical reference cavities, coupled with the high gain of the PDH feedback loop and the low frequency of optical noise sources, these circuits can be operated at ~100 kHz bandwidths and integrated using mW level power consumption Bi-CMOS circuits. Applying these stabilization and linewidth reduction techniques to integrated multiple wavelength Tx and LO sources provides a unique opportunity to bring coherent WDM into the DCI, offload DSP functions like carrier and phase recovery and avoid high power electronic mixers and digital circuits used in traditional OPLL and EPLL coherent receivers. The goal of FRESCO is to achieve 2 pJ/bit for transmit and 2 pJ/bit for receive over DCI distance (< 2km). In principle it is possible to apply this approach or a subset of the technologies to longer reach links, and this is an area that requires further investigation over extended fiber distances.

The FRESCO transceiver, shown in Figure 10, is based on a shared ultra-stable, spectrally pure WDM source for the Tx and LO carriers. The shared optical source consists of a silicon photonic tunable laser [37] that serves as the pump for a silicon nitride SBS laser [35]. The ultra-narrow linewidth SBS laser emission is locked to an ultra-stable optical reference-cavity [36] that is used to pump a nonlinear Kerr soliton optical frequency comb (OFC) [38]. The ultra-low linewidth, ultra-stable WDM carriers serve as both Tx and LO WDM source. Highly integrated silicon photonics [39] are used for QAM WDM modulators and receivers. In order to achieve our FRESCO project goals of 1.6 Tbps per wavelength links, we chose a starting design point as coherent QAM, with baud rates of 64 and 72 GBd and amplitude-phase modulation of 64- to 512-QAM. These baud rates and constellation sizes are not intended to match industry standards, rather we are using them to drive our technologies. All chip sets will be implemented using foundry compatible silicon photonic and silicon nitride processes. The FRESCO transceiver is designed to be co-located with the switch ASIC and future designs will investigate coherent QAM electrical drivers that directly interface to the silicon photonic drivers, as well as transimpedance amplifier (TIA)-free CMOS designs for the receiver. Areas of ongoing study include power efficiency for each transceiver stage (e.g. tunable SiPh laser to SBS laser, SBS lasers to OFC). Today, non-integrated versions require approximately 10 mW on-chip optical power for SBS threshold with ~ 50% slope efficiency. Conversion efficiency for the discrete OFC is dependent on many parameters and typically falls around 0.1% for a non-optimally engineered Kerr frequency comb, a number we expect to improve by limiting the number of comb lines to the WDM channel count and other approaches including QD mode locked lasers (QD-MLL)[40]. Integration using mode transformers between stages will greatly improve the overall efficiency. There is the potential also to use highly efficient, high output power, WDM quantum dot semiconductor optical amplifiers (QD-SOAs)[41] to boost OFC comb power and transceiver output.

The principle of frequency stabilized coherent communication is illustrated by a loose analogy in Figure 11. Two aircraft carriers act as large masses that dampen water movement and other environmental fluctuations. Two sailboats (with sails lowered), each tethered to an aircraft carrier, have their motion dampened by the large masses. On one sailboat is a person with a thread attempting to thread the needle held on the other sailboat. While still a difficult task, the amount of energy used by the people on the boats used to thread the needle will be much less than if the sailboats were free and not tethered to the large masses. On the right side of Figure 11, the ultra-high Q optical reference μ-cavities play the role of large

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thermal/optical masses stabilizing the Tx and LO tunable laser frequencies. The signal and LO require much less energy to align their intermediate frequency and lock their phase after photodetection using low bandwidth electronics. The FRESCO power reduction benefit is realized when the power consumption of the circuits used to stabilize the lasers and perform the final stabilized frequency/phase lock, is much less than the energy required to lock unstablized lasers using DSP type approaches

A FRESCO link is illustrated in Figure 12. The transmit constellation phase noise is extremely well defined, and over engineered relative to traditional QAM laser linewidth requirements, but not at the expense of excess power consumption due to the high efficiency of PDH optical reference cavity stabilization. The cost, complexity, and energy of the stabilized shared WDM source is amortized over all WDM channels of a FRESCO transceiver and link. The SNR of the transmit constellation symbols for each wavelength is set in part by the WDM linewidth per channel, which is on the order of 10s of Hz phase noise and ultra-low fractional-frequency stability (e.g. $\sim 10^{-14}$), providing an extremely clean, stable constellation and symbol space.

At the receiver, an LO with comparable phase noise and fractional frequency stability mix with the transmitted signal to produce a constellation with heterodyne IF (or homodyne) with an extremely low RF linewidth (e.g. < 40 Hz) and residual phase error comparable with DSP phase recover (e.g. $< 3 \times 10^{-4}$ rad^2). Both the Tx and LO lasers are stabilized using mW level power consumption, low bandwidth PDH circuits and a mW level power consumption, low bandwidth optical frequency stabilized phase locked loop (OFS-PLL).

Issues to be addressed include manufacturing and environmental variations in OFC comb frequency tooth spacing between transmit and receive OFCs. It is preferable to manage two stabilized combs by monitoring a single IF beat note. If the fabrication or tuning tolerance between OFCs produces comparable IFs, variations can be managed through simple electronic filter tuning. If the IF is larger or out of range, a separate sideband modulator can be supplied for channels out of spec, allowing the frequency to be offset within some range independently for each channel. Ideally, we are investigating the potential to use one OFS-PLL for all WDM channels on a fiber or on a subset of wavebands. However, to at the start of this research there will be one OFS-PLL per wavelength. In terms of dynamic range of the transmit and receive PDH stabilization loops and the final OFS-PLL loop to lock those together, we plan to use a simple temperature "kicker" that monitors the beat frequency, and apply a small current pulse to move the direction of the reference cavity drift, where the monitoring is set with thresholds within the OFS-PLL dynamic range.

V. FRESCO Technologies

Examples of the FRESCO integration and component technologies are shown in Figure 13. The high power extended cavity silicon photonic tunable laser [37] and silicon photonic transmitters and receivers [39] are fabricated using wafer-scale CMOS compatible heterogenous integration processes [42]. The ultra-narrow (sub-Hz intrinsic) linewidth silicon nitride SBS laser [35] and Nonlinear Kerr soliton optical frequency comb (OFC) [38] are integrated using ultra-low loss wafer-scale CMOS compatible silicon nitride [43] and tantalum pentoxide [44] waveguide platforms. The optical reference μ-cavity is a bulk, fused-silica cylinder with super-polished, low-loss reflection coatings to realize a Q-factor of ~ 1 Billion [36]. In the future, it is envisioned that the bulk optic reference cavity will be closely integrated with the waveguide components and eventually will be implemented in a waveguide.

VI. Summary and Future Prospects

As Hyperscale data centers become prevalent, switch ASIC chips, the engines of the Data Center Interconnect (DCI), will grow in capacity from 12.8 Tbps today to 102.4 Tbps and beyond, straining engineerable fiber optic interconnect solutions and their cost and energy resources. We have described FRESCO, a new approach that leverages the properties of spectrally-pure highly-stable light developed for large scale physics experiments, to bring ultra-high capacity long-haul coherent optical solutions into the DCI without energy consuming electronics. FRESCO is designed to bring coherent WDM into the DCI and address power consumption and engineering limitations that will exist as switch ASIC capacity scales to 102.4 Tbps and beyond.

The FRESCO transceiver is based on a shared ultra-stable, narrow-linewidth laser and optical frequency comb to deliver DSP-free coherent carrier and phase recovery with low-power, low-bandwidth control loops supporting multi-Tbps channels. FRESCO utilizes highly integrated silicon photonic and silicon nitride transceiver technology to provide a co-packaged solution. Frequency and linewidth narrowing techniques, typically the hallmark of large scale science, are integrated to the chip scale to bring ultra-narrow linewidth, ultra-stable WDM coherent sources to address power consumption issues associated with DSPs and high bandwidth analog and high frequency digital electronics for analog OPLL and EPLL.

We have described the frequency noise and stability characteristics that need to be considered when engineering an ultra-low linewidth, ultra-stable, coherent QAM link and the low bandwidth low power feedback stabilization that is employed for the Tx and LO laser and optical frequency combs, to allow mW level, order 100 kHz bandwidth feedback loops, to perform optical frequency stabilized carrier and phase locking (OFS-PLL) for WDM Tbps channels. Other issues that remain to be addressed in the future to further lower power of coherent WDM include elimination of transmitter DACs, utilizing ultra-narrow linewidth and stability to relax the requirements on receiver ADCs and low energy CDR.

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